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Multi-Objective Comparative Analysis of Active Modular Rectifier Architectures for a More Electric Aircraft †

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Abstract: Aircraft electrification requires reliable, power-dense, high-efficient, and bidirectional rectifiers to improve the overall performance of existing aircrafts. Thus, traditional bulky passive rectifiers must be substituted by active rectifiers, satisfying the requirements imposed by up-to-date standards. However, several challenges are found in terms of power controllability, due to the standardized passive rectifier-based operating conditions. This work presents the implementation of an active rectifier modular architecture for aircraft applications. An analysis of the technical difficulties and limitations was performed and three innovative modular architectures are proposed and designed. In order to find the most suitable architecture, a comparison framework is proposed, focusing on efficiency, volume, and reliability parameters. From the comparative analysis, it can be concluded that the two-stage configuration architecture is a good solution in terms of semiconductor life expectancy and low volume. However, if converter redundancies are required, the single-stage with STATCOM configuration is an excellent trade-off between low volume, redundancy, and cost-effectiveness.

Keywords: more electric aircraft; electric power system architecture; aerospace generation drives; AC–DC converter; three-phase rectifier; HVDC; power factor correction (PFC)

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1. Introduction

Higher efficiency, fuel saving, global warming emission reductions, and lower maintenance costs are, among others, crucial benefits of encouraging aircraft electrification [1]. Since conventional aircraft are equipped with bulky hydraulic, pneumatic, and mechanical systems, the more electric aircraft (MEA) concept pretends to replace these non-propulsive systems with more efficient and compact electrical systems [2–4]. Compared to conventional systems, electrical systems present numerous benefits, such as higher power density, reliability, maintainability, performance, and lower costs [1,2]. However, the more the aircraft is electrified, the higher the complexity of the power system [1,4,5].

In this context, promoting highly-efficient and high power density aircraft electric power system (EPS) architectures has become a research focus [4,5]. A strong trend in the MEA power system development is related to the "single-bus" approach presented in Figure 1a [3,4,6]. This concept is based on a single high voltage DC (HVDC) primary distribution bus to interface all the loads and sources of the aircraft. Consequently, the issues related to AC distribution, such as a higher number of cables and weight, or reactive power compensation, are avoided, and a high power density EPS is achieved.

In the existing MEA power systems, the HVDC bus is generated by a passive multipulse system named the auto-transformer rectifier unit (ATRU) [1,3,6]. This system is

featured by its low costs, high reliability, and simplicity [7]. Its low power density and non-controlled output voltage, though, demand the development of new technologies that satisfy the operating, power quality, and harmonic requirements of aviation standards, such as MIL-STD-704F or DO-160G [8].

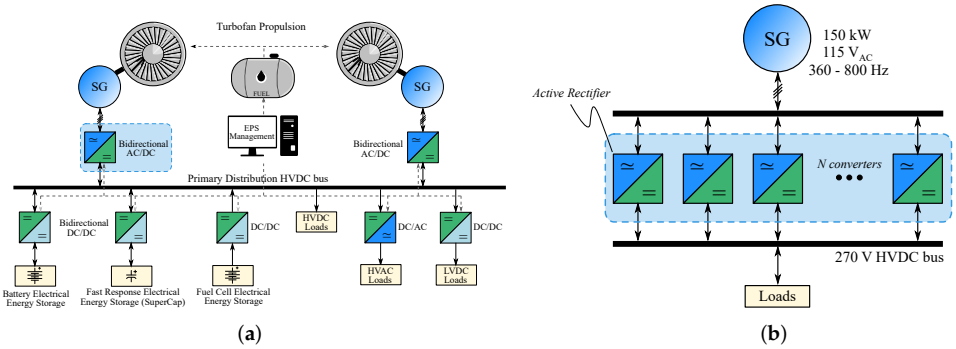


Figure 1. Examples of (**a**) a simplified electric power system architecture based on "single-bus" MEA topology, and (**b**) the proposed simplified active modular converter architecture.

Therefore, in encouraging the implementation of the EPS in Figure 1a and the replacement of the bulky unidirectional passive ATRU, active power factor correction (PFC) rectifiers are considered as potential options to encourage aircraft electrification [2,3,6,9]. Compared to passive solutions, active PFC converters are featured for improved power quality and reduced weight and volume. Additionally, continuous progress under the MEA concept not only requires the inclusion of advanced power electronic designs, but also innovative concepts, such as the electrification of the propulsion system employing bidirectional power flow rectifiers for future aircraft power systems (see Figure 1a) [3,10–14]. The achievable power, efficiency, power density and reliability/availability of these active rectifier topologies are, however, currently restricted by state-of-the-art technologies [9].

In this context, it is believed that implementing wide band gap (WBG) semiconductor technologies will be advantageous, due to increased converter efficiency. Among the benefits provided by WBG devices, such as silicon carbide (SiC) or gallium nitride (GaN), over traditional silicon devices, a lower resistance and a faster switching capability can be found [13,15–21]. Therefore, apart from achieving a lower conduction and switching losses, other features, such as a higher efficiency, lower cooling effort, and a reduced volume for passive elements can be expected from WBG-based converters. Additionally, the higher and more efficient switching speed capability can be accomplished with lower difficulty power quality requirements, without employing bulky filters.

However, one clear difficulty in implementing active rectifiers is found in existing aviation standard requirements, which are based on passive ATRU operations. The present-day input/output voltage requirements, being 115 V_{AC} (phase-to-neutral) to 270 V_{DC} or 230 V_{AC} (phase-to-neutral) to $\pm$ 270 V_{DC}, depending on the manufacturer, result in controllability limitations for active rectifier systems. In addition, among the major challenges, the design of an active power converter rated at a high power, in order to supply the increasing, electrified aircraft power demand, is considered to be a complex task [4,9,13]. Thus, parallel operation and modular converter approaches are encouraged, aiming, for instance, to achieve an increased overall architecture power rating with a high degree of redundancy [9–11,22]. One example is presented in Figure 1b, in which a viable design is assumed to be achieved without compromising the safety and reliability criteria while fulfilling the aircraft operational requirements [10].

Several active rectifier designs and comparative analyses can be found in the literature for MEA applications [5,7,14,19,23–27]. These research works present different studies about the topology selections, power loss analyses, and/or input filter designs. However, they do not fulfil the currently standardized passive rectification operating requirements

or provide all of the emerging requirements, such as bidirectional power flow capability. Besides, no rectifier architecture structure is defined.

The suitability of active rectifiers and a comparisons among different topologies in MEA applications are presented in a previous work by the authors [28], in which a two-level boost, three-level NPC, and T-type are compared and benchmarked with an ATRU. As a result, two-level boost topology had the highest efficiency and high power quality at relatively higher switching frequencies due to implementation of WBG technology. In this work, we propose the implementation of a two-level boost active rectifier in an active modular architecture structure, with the aim of finding the most suitable architecture for the defined MEA application. Based on a technical approach, we performed an analysis of the difficulties and limitations of implementing active modular architectures, from which three different architectures are proposed. We present the design of each active modular architecture and propose a wide comparison framework, focusing on efficiency, power density (referred to volume), and reliability, again, with the aim of identifying the most suitable architecture.

Based on previous work, the suitability of active rectifiers and a proposal of three converter configurations are presented in Section 2. An extended comparison framework is described in Section 3, aiming to establish the most suitable active modular architecture based on the different converter configurations, focusing on the overall architecture efficiency, volume, and reliability. The converter configurations were then integrated into an active modular architecture structure. The design criteria of each architecture is presented in Section 4 and comparisons among them are provided in Section 5. Finally, we present the conclusions of this work in Section 6.

2. Suitability of Active Rectifier Topologies in MEA

2.1. Application Requirements and Operating Scenario

Research surrounding highly-efficient and high power density EPS encourage implementation of active modular converter architectures. In particular, using active rectifiers (and architectures) in MEA starter-generator (SG) applications is a key concern due to the existing input/output voltage operating scenarios based on the performances of passive rectifiers. Thus, in order to establish the operating scenarios of active rectifiers, and considering the power system weight analysis in [29], the 115 V_{AC} to 270 the V_{DC} rectification scenario was selected (as in the case of Airbus A380, where a 150 kW power per SG was specified) [3]. Thus, the application requirements described in DO-160G [30] were assumed and are summarized in Table 1. In addition, the expected future design target for the year 2025, in terms of efficiency, is also considered due to the acknowledged impacts in the aviation industry [31].

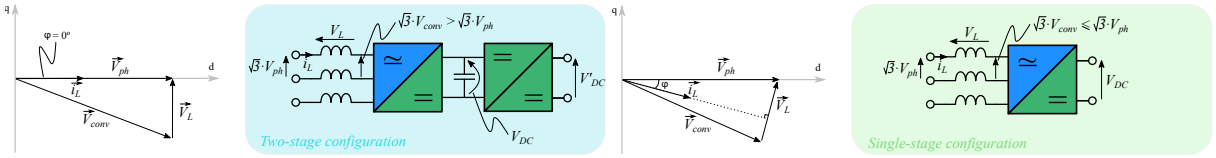
Table 1. Application requirements and future targets.

Parameter	Value
Nominal phase RMS voltage, V_{ph}	115 V
Steady state phase RMS voltage	100–122 V
Steady state frequency, f	360–800 Hz
Power factor, PF	0.85–1
Current total harmonic distortion, THD_i	$\leq$3%
Nominal DC voltage, V_{DC}	270 V
Steady state DC voltage	250–280 V
Architecture power rating	150 kW
Targeted efficiency	$\geq$97%

2.2. Evaluation and Limitations of Active Rectifier Topologies

From Table 1, special attention should be given to the defined steady state output voltage between 250 V_{DC} and 280 V_{DC} when the input phase root mean square (RMS)

voltage, V_{ph}, is 115 V_{AC}. This output DC voltage range, typical for passive ATRU operation, is identified as an uncontrolled output voltage range for active rectifiers (either buck-type or boost-type) when operating at unity power factor (PF) [7,8]. Thus, in an attempt to cover the uncontrolled voltage range with active rectifiers, an additional DC/DC stage could be added to the active rectifiers to achieve an output voltage of 270 V_{DC} [8]. This concept, considered in this work as a *two-stage converter configuration* is represented in Figure 2a.



(**a**) (**b**)

Figure 2. Phasor diagram and converter configuration at (**a**) two-stage and unity PF operation, and, (**b**) single-stage and lower than unity PF operation.

One distinct perspective in adding the DC/DC stage to achieve the required 270 V_{DC} can be found for active boost-type rectifiers, whose output voltage, V_{DC}, is defined as [32],

$$V_{DC} = \frac{2\sqrt{2}\,V_{conv}}{m} \tag{1}$$

where m refers to the modulation index, and the converter terminal RMS input phase voltage is defined as V_{conv}. Thus, for a maximum theoretical linear m of 1.15 [32], a *single-stage* rectification possibility arises if $V_{conv} \leq 109\ V_{AC}$ as depicted in Figure 2b. Consequently, in order to replace the passive ATRU for an active boost-type rectifier while fulfilling the DO-160G operating requirements, two different scenarios are possible [28]:

1. *Two-stage configuration*: considering the best PF operating condition case in Table 1, the active rectifier presents unity PF operation, and, according to the phasor diagram in Figure 2a, $V_{conv} > V_{ph}$. Thus, the rectifier output voltage ($V_{DC} > 282$ V) does not fulfil the application requirements and a posterior DC/DC conversion is required to achieve the specified output 270 V_{DC}, expressed as V'_{DC}.
2. *Single-stage configuration*: considering the worst PF operating condition case in Table 1, the active rectifier performs at PF = 0.85 lagging and, therefore, $V_{conv} \leq V_{ph}$ condition is fulfilled, as depicted in Figure 2b. Therefore, no additional converter is required downstream for achieving the targeted 270 V_{DC}.

From two operating scenarios presented above, a topology assessment is performed based on the methodology proposed in [33] to demonstrate the suitability of active rectifier topologies in MEA applications [28]. The potential active rectifier topologies are selected from the literature, being two-level boost [7,8,14,23,34], NPC [14,35,36] and T-type [23,35] topologies, and they are benchmarked with an ATRU model, based on [7,37]. Regarding the aviation context, the assessment focuses on efficiency, power density, reliability, weight, and volume characteristics, which, indeed, are partially related by the topology, switching frequency, and power quality. Since a higher switching frequency is desired to reduce the input filter volume, the implementation of WBG semiconductor technology is encouraged in the analysis, aiming for a high converter efficiency and power density. Hence, for the specified operating scenario and the power rating under comparative study, *ST-SCTW90N65G2V* SiC metal-oxide-semiconductor field-effect transistor (MOSFET) and *GeneSiC-GC50MPS06-247* Schottky diode semiconductors were selected as no lower blocking voltage rating SiC semiconductors were found in the market, and, GaN devices do not reach a current rating as high as SiC devices. More details of the active topology selection, comparison procedure, and numerical results can be found in [28].

From the analysis results, in a previous work [28], it was concluded that, among the active rectifier topologies, two-level boost configurations were preferred for this application

due to their relatively high efficiency, low filtering efforts required at relatively higher switching frequencies (comparable to three-level topologies at ≈80–100 kHz), the low number of power devices, and simplicity. Concretely, single-stage configuration presents greater potential in terms of efficiency and simplicity. Furthermore, this configuration not only presents a lower number of power devices but also a decreased average junction temperature compared to two-stage configuration due to the higher amount of power losses per semiconductor dissipated by the DC/DC stage. Hence, a higher reliability can be expected from the single-stage configuration due to the lower thermal stress, lower blocking voltage, and lower number of power devices [38]. However, operating at a PF < 1 implies polluting the grid with reactive power. Since unity PF is preferred at the connection point to the grid, to avoid reactive power handling and achieve a higher efficiency, both single-stage and two-stage configurations are assessed at this operating condition.

2.3. Proposed Converter Configurations for Operating at Unity PF

As previously mentioned, the two-stage configuration (presented in Figure 3a, named from now on as $2L_2$ configuration) operates at unity PF. Although this concept appears to be a relatively simple configuration, the overall converter efficiency and power density are penalized by the downstream second power stage. In fact, as stated before, the expected higher thermal stress presented on the second power stage might also lead to a reduced converter lifetime.

In the case of the single-stage configuration, the lowered PF operation could be corrected by means of an input capacitor bank. This configuration concept, named $2L_C$, and represented in Figure 3b, not only achieves unity PF operation at the grid connection point, but also improves the filtering characteristic, providing a second order LC filter. Thus, the added capacitor bank should be designed to compensate the reactive power requested in the whole grid frequency range, i.e., from 360 to 800 Hz. The downside of designing the capacitor bank for the minimum reactive power request operation, which is at 360 Hz, is that the operating PF is lowered at higher frequencies as a result of the needless amount of the capacitive current delivered.

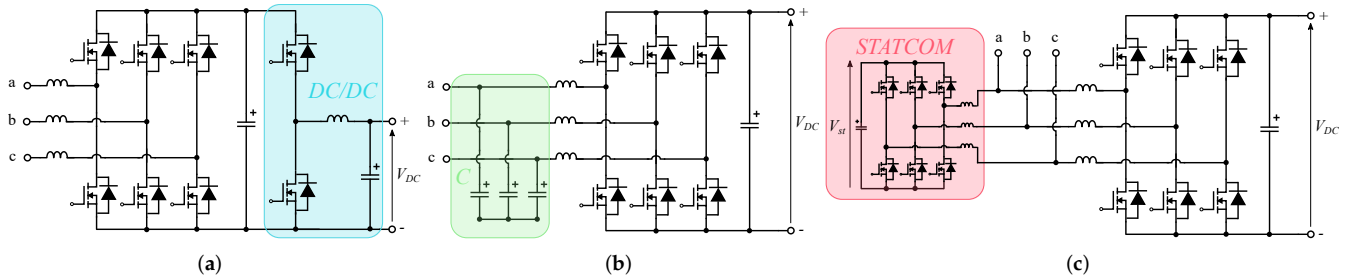


Figure 3. Schematics of the (**a**) two-stage $2L_2$ and the single-stage, (**b**) $2L_C$, and (**c**) $2L_{st}$ configurations.

In order to reduce the excessive capacitive current delivered by the capacitor bank at high grid frequencies, an additional converter configuration is considered, which replaces the input capacitor bank by a static synchronous compensator (STATCOM). Among the benefits of this configuration concept, depicted in Figure 3c and named as $2L_{st}$, the STATCOM, which is disconnected from the distribution bus and establishes its own higher DC voltage bus, provides the necessary amount of reactive power required by the active rectifier to achieve a single-stage operation throughout the operating grid frequency range. Consequently, no additional reactive power is handled as in $2L_C$ configuration and higher efficiency values might be achieved owing to a higher number of power converters. The additional converters could provide a higher redundancy degree to the active rectification architecture if the STATCOM could also operate as an active rectifier in case of a rectifier failure.

Although $2L_2$, $2L_C$, and $2L_{st}$ configurations achieve unity PF on the connection point to the grid, the selection of the most suitable converter configuration for implementing an active modular architecture is not straightforward. Due to the different attributes that surround each topology, a comparative analysis is required among the different architectures, which focuses on critical aspects related to the aviation context [31,39], being efficiency, power density, reliability, and the proper architecture configuration design.

3. Comparison Framework for Active Rectification Architectures

3.1. Efficiency Estimation

The efficiency calculation of the different architectures was based on the proposed evaluation methodology in [33]. Based on the application requirements in Table 1, and the simulation models, the on-state conduction power losses, P_{cond}, and switching power losses, P_{sw}, are evaluated according to the SiC MOSFET *ST-SCTW90N65G2V* semiconductor characteristics and the converter operating conditions. From the device data sheet, the worst case 200 °C maximum junction temperature figures are harnessed for the power losses estimation to provide a conservative approach to thermal dissipation and reliability modeling [40].

Considering the aggregate of all the semiconductor power losses, the overall architecture efficiency, η, is calculated as

$$\eta = \frac{P_{load}}{P_{load} + \Sigma(P_{cond} + P_{sw})} \cdot 100 \tag{2}$$

where P_{load} refers to the overall architecture transmitted active power; hence, 150 kW based on the Airbus A380 model [1,3]. We should mention that, from the application requirements of Table 1, a minimum of 97% efficiency was targeted for the active rectification architecture.

3.2. Volume Estimation

The cooling system and passive elements are the main contributors to the overall converter weight and volume [39]. Estimations of the converter volumes can be performed based on proportional parameters, such as the stored energy for passive components or the thermal resistance for the heat sink [39,41,42]. Thus, a comparative approach of the power density of the converters and, hence, architectures, could be obtained.

3.2.1. Cooling System Volume

According to [42], the volume of a converter heat sink, Vol_h, is inversely proportional to its thermal resistance as,

$$Vol_h = k_h \frac{N_{conv}}{R_{th_{h-amb}}} \tag{3}$$

where k_h corresponds to the volumetric resistance of the specific heat sink type, and $R_{th_{h-amb}}$ represents the thermal resistance from the heat sink to ambient. With the aim of considering the volume of the overall architecture cooling system, the number of converters was introduced in the formula as N_{conv}. Since the same heat sink type is assumed for the comparative analysis, the volumetric resistance can be neglected for comparative intentions.

From the semiconductor power losses evaluation, a thermal model was employed, considering the following assumptions:

- For safety reasons, the achievable maximum junction temperature was defined as 15 °C lower than the data sheet temperature and, hence, was limited to 185 °C.
- Water-cooling was assumed in order to achieve a high power density architecture. Based on the cooling system specifications of "IQ-evolution" [43], a temperature jump from heat sink to ambient, ΔT_{h-amb}, of 15 °C is defined.
- An ambient temperature of 70 °C is assumed according to the worst case temperature in [30].

- Due to the high frequency of the SG voltage, the junction temperature ripple of the power semiconductor devices is negligible. Thus, instead of the transient impedances, only the thermal resistance is considered in this comparison.

Thus, based on the considered steady-state thermal model and the converter total losses, the thermal resistance from the heat sink to ambient is calculated as,

$$R_{th_{h-amb}} = \frac{\Delta T_{h-amb}}{N_{dev} \cdot (P_{cond} + P_{sw})} \tag{4}$$

being N_{dev} as the number of semiconductors in each power converter configuration.

3.2.2. Volume of the Passive Components

In terms of passive elements, in [39,41] the volume of a passive element, Vol_p, is proportionally related to its stored energy, E:

$$Vol_p = k_p \cdot E \tag{5}$$

where k_p represents a volumetric coefficient of the passive element. Since this coefficient depends on the manufactured passive element structure and type, assumed to be equal for each architecture, the provision of a simplified analysis was neglected. In fact, even if different geometric structures and materials were used to manufacture passive elements, the dependency of volume with energy was verified in practice, in [41].

The following expressions represent the stored energy for a capacitor, E_C, and an inductor, E_L:

$$E_C = \frac{1}{2} C \widehat{V}^2 \tag{6}$$

$$E_L = \frac{1}{2} L \widehat{i_L}^2 \tag{7}$$

where C and L represent the capacitance and inductance values, respectively; $\widehat{V}$ expresses the capacitor peak voltage value, and $\widehat{i_L}$ the peak current value flowing through the inductor.

3.3. Reliability Estimation

Power semiconductors are recognized as the most fragile components in terms of power converter reliability [38,44,45]. The failure rate of these components is commonly correlated to the *bathtub curve* describing the different stages of the component lifetime [45]. In the early stages of the lifetimes of the devices, the failure rate is high due to the production quality fluctuations.

Regarding the useful life of the power device, its failure rate is considered constant and related to cosmic ray-induced failures [45]. The origins come from highly-energetic atomic particles, which collide with the atoms of the power device, causing electric charges to be deposited in the device. These charges, combined with high electric fields during a reverse blocking mode may result in a streamer of electrons producing a sudden device destruction due to the short-circuiting of a phase leg [40].

In the last stage of the lifetime of the power device, failures are caused by wear-out of the chip and its package, known as wear-out failures [45]. These failures occur as a result of the electrothermal fatigue caused by the thermal cycling of the devices and the time-varying mission profile of the converter [38,40,46]. The mission profile represents all relevant conditions that the converter will be exposed to in the intended application, i.e., the altitude, ambient temperature, and output power, so that the stress that withstands the power device can be estimated. Due to the lack of a mission profile representative of aircraft applications, in this work, a simplified mission profile based on the one described in [40] is adopted. This way, it is considered a 1-hour flight at cruising altitude (30,000 ft) in which the active rectifiers operate at nominal power. It is also assumed that the aircraft performs six flights per day throughout the whole year.

3.3.1. Cosmic Ray Failure Rate

Typically, the reliability of a component related to the cosmic ray-induced failures is expressed by its failure rate, λ, being $\lambda = 1\,\text{FIT} = 1/10^{-9}\,\text{h}$. A failure in time (1 FIT) corresponds to, statistically, one failure per one billion hours of operation. The failure rate value of a power device is mainly influenced by its reverse blocking voltage and the cosmic ray flux intensity [40,45,47]. In this work, the architecture failure rate estimation employed was based on the International Electrotechnical Commission (IEC) standard 62396-4 (referenced for high voltage power devices in aircraft applications) [40].

Based on the universal curve in [47–49] and the experimentally tested breakdown voltage in [50], the FIT/cm^2 of each MOSFET was calculated (applying a curve fitting algorithm) for every architecture configuration. Afterwards, considering that the neutron flux intensity at 30,000 ft (mission profile cruise altitude) is higher than at sea level conditions, i.e., universal curve conditions, the FIT/cm^2 value is scaled using the altitude factor in [51,52]. Thus,

$$\lambda_h = \lambda_0 \cdot exp\left(\frac{1 - \left(1 - \frac{h}{44300}\right)^{5.26}}{0.143}\right) \tag{8}$$

where λ_0 refers to the FIT/cm^2 value obtained in the universal curve at sea level (see Table 2), and, λ_h the estimated value at cruising altitude, h.

Table 2. Sea level FIT/cm^2 rates from the universal curve considering a semiconductor breakdown voltage of $V_{bd} = 1151$ V.

Configuration	V_{ds}	λ_0
$2L_C$ & $2L_{st}$	270 V	$1.74 \cdot 10^{-4}$
$2L_2$	312 V	$3.38 \cdot 10^{-5}$
$2L_{st}$	459 V	0.0304

In order to obtain the power device FIT value, λ_h is multiplied by the power device chip area. However, since the same power device is assumed in all of the configurations, the FIT/cm^2 can be employed for comparison purposes. Additionally, the calculated FIT/cm^2 rates are valid for a semiconductor during blocking mode. Therefore, a scaling factor should be applied that corresponds to the percentage of the time spent in blocking mode [40]. Thus,

- A 50% for the power devices of the AC/DC stage;
- A 13.5% and 86.5% for the upper and down power devices in the DC/DC stage of $2L_2$ converter, respectively.

Once the FIT/cm^2 value of each power device is calculated and scaled, λ'_h, the FIT value for the whole architecture λ_{arch} is obtained summing up the scaled FIT values of all the devices in the architecture:

$$\lambda_{arch} = \Sigma\, \lambda'_h \tag{9}$$

3.3.2. Wear-Out Performance Analysis

Caused by the cyclic power losses, thermal cycling is identified as the most important stressor that affects reliability in terms of wear-out failure [38,44]. Moreover, since the thermal stress depends on the power device mission profile previously described, a mission profile-based reliability evaluation is applied in this work [38,40,44].

Based on the previous calculations on average power losses in Section 3.1 and as a consequence of the employed electrothermal model, the average junction temperature of the different power devices was determined. Thus, in order to determine the number of kilocycles to failure of the power devices due to thermal cycling, N_f, a lifetime model was used, presented in [44,46] for MOSFET power devices, based on a Coffin–Manson Law.

The employed lifetime model, already used in literature for the evaluation of SiC MOSFET lifetimes [53–55] is expressed as,

$$N_f = \alpha \cdot (\Delta T_{j-amb})^{-m} \tag{10}$$

where ΔT_{j-amb} represents the temperature rise from ambient to junction, and, α and m are fitting parameters defined as $5 \cdot 10^{11}$ and 5.3 in [46], respectively.

Note that the obtained result in (10) concludes a fixed value for the number of cycles to failure. However, there are some uncertainties in the performed analysis that should be considered, such as [38,40,44]:

- The MOSFET lifetime model and the fitting parameters employed derived from testing data in [46];
- The thermal and electrical parameters related to the power devices, which could vary due to the manufacturing process and semiconductor technology; or
- The simplified mission profile, which could vary with the climate change and load conditions.

As a consequence of the existing uncertainties, a sensitivity analysis was also performed by means of a Monte Carlo simulation, so that the reliability could be expressed in statistical values rather than fixed. This way, the Monte Carlo simulation was based on a 5% variability and 10^5 population samples [44]. Afterwards a standard distribution fitting was applied and the cumulative distribution function (cdf) of each device, $F_{dev}(t)$ was extracted. Thus, considering a series connected reliability model in which any device failure leads to the failure of the architecture, the architecture cdf, F_{arch}, is calculated as,

$$F_{conv}(t) = 1 - \Pi(1 - F_{dev}(t)) \tag{11}$$

$$F_{arch}(t) = 1 - \Pi(1 - F_{conv}(t)) \tag{12}$$

where $F_{conv}(t)$ represents the converter cdf. Examples of the architecture, converter, and device cdf are presented in Figure 4a. In order to acquire a high reliability indicator for the comparison [38,39], the B_1 cycle to failure parameter is extracted from the resulting architecture unreliability curve, $F_{arch}(t)$. This parameter represents the number of repeat mission profiles after which the architecture survives at 99%, which, after applying the mission profile data (cycles per year), can be estimated in a period of years (see Figure 4b).

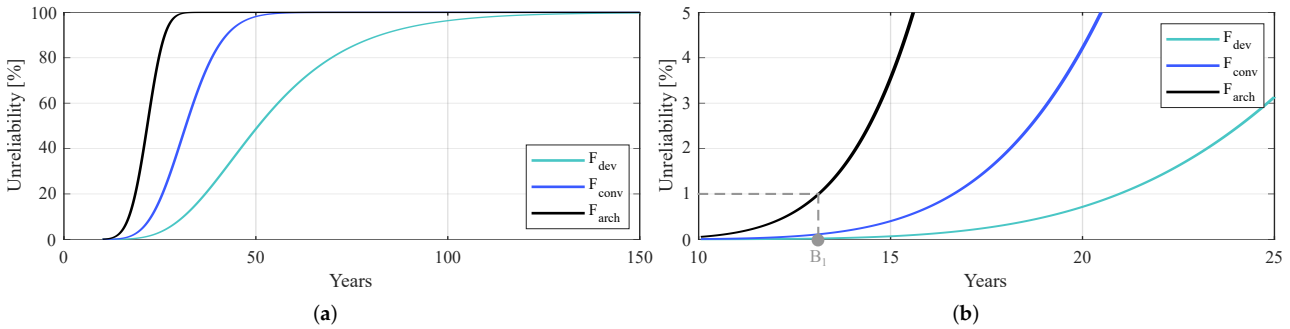


Figure 4. (**a**) Unreliability curves for an architecture formed identical converters based on a single device type, and, (**b**) zoomed curves where the B_1 parameter is presented.

4. Converter Configuration and Architecture Design

Aiming to design the architectures related to $2L_2$, $2L_C$, and $2L_{st}$ converter configurations, the following concepts were considered:

- The presented architectures were designed to fulfil the efficiency targets and operating requirements in Table 1 as well as the power quality and harmonic requirements, both low-frequency (LF) and high-frequency (HF), in DO-160G [30].

- The operating PF of the power converters were analyzed by the equation describing the phase diagrams in Figure 2, being,

$$V_{conv}^2 = (V_{ph} - V_L \cdot \sin(\varphi))^2 + (V_L \cdot \cos(\varphi))^2 \tag{13}$$

where $\cos(\varphi)$ refers to the operating PF; and, V_L symbolizes the inductor RMS voltage, which can be expressed as,

$$V_L = 2\pi f L i_L = 2\pi f L \cdot \frac{P}{3V_{ph}\cos(\varphi)} \tag{14}$$

being, f the SG frequency in Table 1, i_L the RMS current flowing through the input filter inductor, and, P the converter nominal power.
We should note that, in the case of $2L_C$ and $2L_{st}$ single-stage configurations (PF < 1), the higher the operating PF, the lower the reactive power to be compensated and, hence, higher efficiency. If (1) and (13) are merged, the maximum operating PF of these topologies can be obtained depending on V_L for a fixed m,

$$\cos(\varphi) = \sqrt{1 - \left(\frac{V_{ph}^2 + V_L^2 - \left(\frac{m \cdot V_{DC}}{2\sqrt{2}}\right)^2}{2\,V_{ph}\,V_L} \right)^2} \tag{15}$$

A graphical representation of (15) is depicted in Figure 5 where the maximum operating PF is represented in a black dashed line for $m = 1.13$.

- Space vector pulse width modulation (SVPWM) pattern is assumed and a maximum $m = 1.13$ to ensure the minimum conduction and blocking times of the employed semiconductor.
- The converter nominal power is defined by means of a thermal analysis based on the steady-state thermal model described in Section 3.2.1. This way, the maximum converter switching frequency is obtained depending on P while maintaining an efficiency result of $\geq 97\%$. The results of the thermal analysis are illustratively represented in Figure 6.

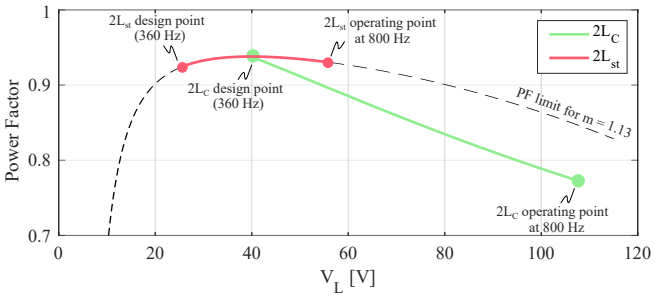


Figure 5. Operating PF of $2L_C$ and $2L_{st}$ converters at nominal power.

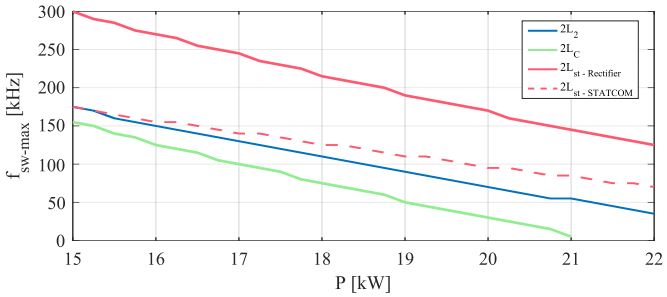


Figure 6. Thermal analysis results for the different power converters.

- Due to restrictive harmonic limitations imposed, a differential LCL filter mode was considered for this application [30,56], where the grid-side inductance corresponded to an assumed SG synchronous inductance of $L_{SG} = 93.5\ \mu H$ (calculated in Appendix A) [57]. Thus, an LC filter was assumed for each power converter configuration. The power quality ($THD_i \leq 3\%$) and harmonic requirements must be fulfilled at the point of regulation (POR), i.e., the point where the active modular architecture is connected to the SG. This concept is represented in Figure 7, where a considered number of synchronized converters, N_{conv}, are connected to the POR. Due to the N_{conv} converter parallelization, the filter inductance and capacitance for the ideal LCL filter of the overall architecture are defined as L/N_{conv} and $C \cdot N_{conv}$, respectively. Thus, based on the transfer function of the equivalent single-phase LCL filter in [58], the transfer function of the architecture LCL filter is defined as

$$H(s) = \frac{i_{SG}}{V_{conv}} = \frac{1}{s^3 \frac{L}{N_{conv}} C N_{conv} L_{SG} + s\left(\frac{L}{N_{conv}} + L_{SG}\right)} = \frac{1}{s^3 L C L_{SG} + s\left(\frac{L}{N_{conv}} + L_{SG}\right)} \quad (16)$$

  Special attention should be paid to the third order filter term in (16), which presents a 60 dB/decade asymptote, since its cut-off frequency is determined by the term LCL_{sg}. Therefore, independent of the number of converters connected to the POR, the cut-off frequency of the 60 dB/decade asymptote is maintained constant. This fact provides the possibility of defining the input filter capacitor for high frequency harmonics filtering without considering N_{conv}.

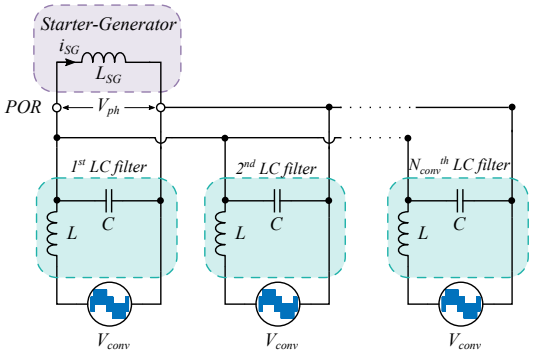


Figure 7. Simplified single-phase architecture equivalent circuit for the high frequency harmonic filtering analysis.

- The dc-link capacitor, C_{link}, of the three configurations is defined for a specific peak-to-peak switching voltage ripple, ΔV_{DC}, according to [59]. Hence,

$$C_{link} = \frac{\widehat{i_L}}{4\, f_{sw} \cdot \Delta V_{DC}} \quad (17)$$

  where f_{sw} represents the power converter switching frequency.

4.1. Two-Stage Architecture-2L$_2$

A simplified example of the considered 2L$_2$ architecture is presented in Figure 8. Since the 2L$_2$ configuration is ideally operating at unity PF, the rectifier output voltage V_{DC}, which is the middle DC bus voltage between AC/DC and DC/DC stages, plays a critical role in the converter design. Under the guise of designing a high-efficient and compact converter, a maximum input inductor voltage of $V_L = 20\,\% \cdot V_{ph}$ is assumed aiming a reduced V_{DC} value and, hence, switching losses. Assuming the worst case operating scenario of DO-160G, where $V_{ph} = 122$ V and $f = 800$ Hz, and applying (1) and (13), a middle DC bus voltage value of 312 V_{DC} is calculated for $m = 1.13$. According to [60], this middle DC bus voltage is then reduced to the targeted 270 V_{DC} by a buck converter employing a duty cycle, D, of 0.865.

With the input/output voltage operating conditions of both power stages specified, a thermal analysis was performed in order to identify the nominal power and switching frequency of the power converter. We should note that, in this configuration, the overall converter performance is also influenced by the DC/DC power stage. Aiming to reduce the relatively high conduction losses, and since a higher thermal stress is presented in the DC/DC stage in this application (as presented in [28]), two parallel DC/DC converters are considered downstream of the AC/DC stage (see Figure 8). Thus, assuming a 10% current ripple and a 2% output voltage ripple, a f_{sw} of 75 kHz and an efficiency of 99.45% is calculated for the downstream stage, so that its passive element volume is significantly reduced [60] and a higher switching frequency of the AC/DC stage can be reached for the same overall converter efficiency.

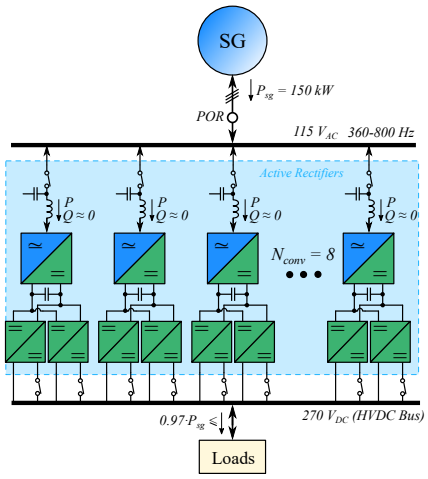


Figure 8. Simplified schema of the proposed active modular $2L_2$ architecture structure.

As a consequence of the DC/DC efficiency result, and aiming for a minimum efficiency of 97% for the overall converter, a nominal power per module of 18.75 kW was obtained and a f_{sw} of the AC/DC stage of 80 kHz considering the worst case operating conditions (see Figure 6), i.e., V_{ph} = 100 V and f = 800 Hz. Thus, the architecture was formed by eight power converters.

With the AC/DC stage switching frequency defined, and aiming for a compact input filter design, a sweep analysis of the current ripple was performed to define both the input filter inductor and capacitor L and C. According to [61], the relation between the input filter inductance, L, and the current ripple, Δi_L, can be defined as,

$$L = \frac{V_{DC}}{6\, f_{sw}\, \Delta i_L} \tag{18}$$

Consequently, the input filter capacitor, C, is designed for harmonic fulfilment. If this design concept is translated to the stored energy by both passive components (using (6) and (7)), the minimum volume input filter design is targeted. In this context, the ripple sweep analysis results, depicted in Figure 9, reveals that the minimum stored energy in the input filter is achieved when a 9% current ripple is targeted assuming nominal conditions, i.e., V_{ph} = 115 V, f_{sw} = 80 kHz and P = 18.75 kW. Thus, the DM filtering results are presented in Figure 10, and the electrothermal analysis results are summarized in Table 3. Aiming to represent the filtering results in terms of power quality, the SG current THD_i is also included.

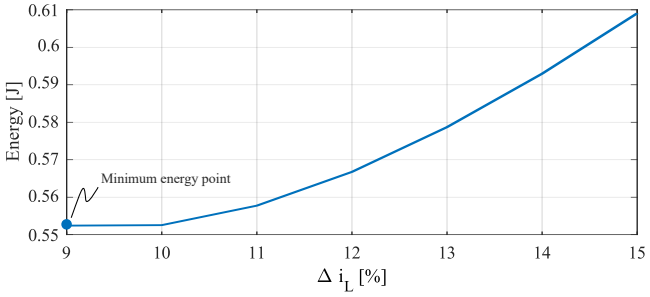


Figure 9. Ripple sweep analysis for calculating the stored energy in the input filter passive elements.

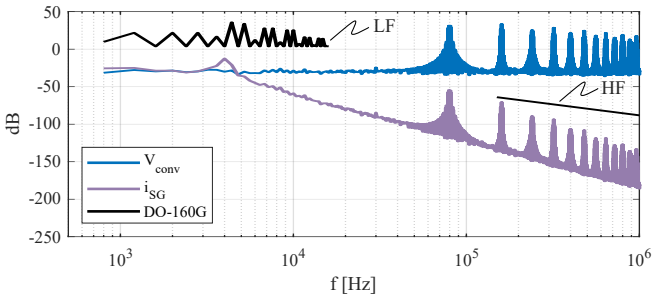


Figure 10. DM input filter results of $2L_2$ architecture for fulfilling LF and HF requirements.

Table 3. Summary of the design parameters of $2L_2$, $2L_C$, and, $2L_{st}$ architectures.

	$\mathbf{2L_2}$	$\mathbf{2L_C}$	$\mathbf{2L_{st}}$
Converter nominal power, P	18.75 kW	16.67 kW	18.75 kW
Nº of SiC MOSFET, N_{dev}	10	6	6
Nº of converters, N_{conv}	8	9	8 + 3
AC/DC switching frequency, f_{sw}	80 kHz	100 kHz	80 kHz
SG current distortion, THD_i	0.05 %	0.11 %	0.13 %
SG inductance, L_{SG}	93.5 µH	93.5 µH	93.5 µH
Input filter inductance, L	94 µH	342.25 µH	191.4 µH
Input filter capacitance, C	18 µF	68.64 µF	19 µF
DC bus capacitance, C_{link}	44.73 µF	42.82 µF	52.18 µF
AC/DC stage output voltage, V_{DC}	312 V	270 V	270 V & 459 V
DC/DC stage output voltage, V'_{DC}	270 V	-	-
DC/DC switching frequency, f_{sw}	75 kHz	-	-
DC/DC inductance, L_{dc}	139.6 µH	-	-
DC/DC capacitance, C_{dc}	1.07 µF	-	-
Maximum temperature rise, ΔT_{j-amb}	55.13 °C	66.28 °C	58.73 °C
Heat sink thermal resistance, R_{h-amb}	0.027 °C/W	0.03 °C/W	0.032 °C/W

4.2. Single-Stage with Capacitor Bank Architecture-2L$_C$

Contrary to the two-stage configuration case, the $2L_C$ architecture benefits from a simplified architecture single-stage structure, as presented in Figure 11. Regarding the power converter design, the higher the operating PF, the lower the reactive power to be compensated by the input filter capacitor banks. Thus, based on (15), and as represented in Figure 5, the maximum PF point (0.938) of the curve is selected as the design point of the power converters assuming 360 Hz grid frequency, that is the minimum. Therefore, by using (14) and introducing $V_L = 39.87$ V, $\cos(\varphi) = 0.938$, $V_{ph} = 115$ V and $f = 360$ Hz, the input filter inductor value can be calculated depending on the converter nominal power, P. The required capacitor value for reactive power compensation can be defined as,

$$C = \frac{i_C}{2\pi f V_{ph}} = \frac{i_L \cdot \sin(\varphi)}{2\pi f V_{ph}} = \frac{P \cdot \tan(\varphi)}{6\pi f V_{ph}^2} \tag{19}$$

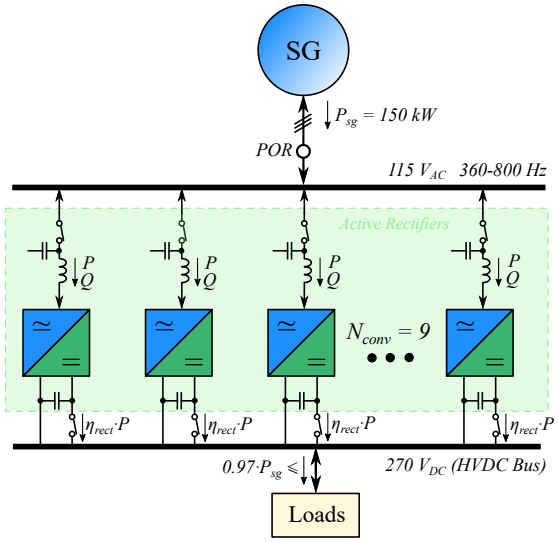


Figure 11. Simplified schema of the proposed active modular $2L_C$ architecture structure.

After performing the electrothermal analysis, considering the worst case operating condition (maximum current), i.e., V_{ph} = 100 V and f = 800 Hz, it is observed in Figure 6 that the desirable 100 kHz switching frequency is achievable at a 16.67 kW converter nominal power. Hence, nine power converters are required for this architecture. Note that, since the capacitor bank is designed for reactive power compensation at a 360 Hz grid frequency, the delivered reactive current at 800 Hz grid frequency makes $2L_C$ converters worsen their operating PF, as far as 0.77 (see Figure 5). The PF at the POR, though, is maintained at unity. Consequently, the design parameters and electrothermal analysis results of the $2L_C$ architecture are calculated for the worst nominal conditions, i.e., 115 V_{AC} and 800 Hz grid frequency, as summarized in Table 3.

We should note that special attention should be paid in this case to the calculated L and C values. The inherent large passive element values required for PF correction are translated into an over filtering effort, as presented in Figure 12, which allows to reduce the switching frequency and increase the converter efficiency. Thus, aiming to squeeze the filtering capability and according to the thermal analysis results in Figure 6, another design possibility could be contemplated by reducing the switching frequency down to 60 kHz and increasing the converter nominal power to 18.75 kW. This design consideration, though, results in a larger amount of energy stored in the passive elements, especially in the dc-link capacitor (see Figure 13). In fact, as presented in Figure 13, the overall stored converter energy, E_{conv}, of the 18.75 kW converter design is expected to be 26.12% larger than the one stored in the 16.67 kW converter design. Therefore, the architecture stored energy is also increased, 12.11%, and the 18.75 kW design possibility is ruled out.

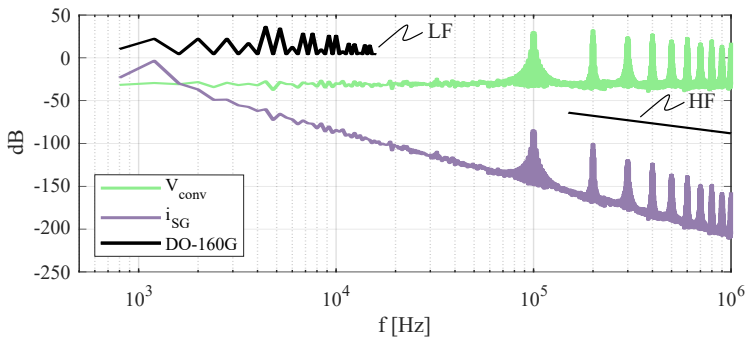


Figure 12. DM input filter results of $2L_C$ architecture for fulfilling LF and HF requirements.

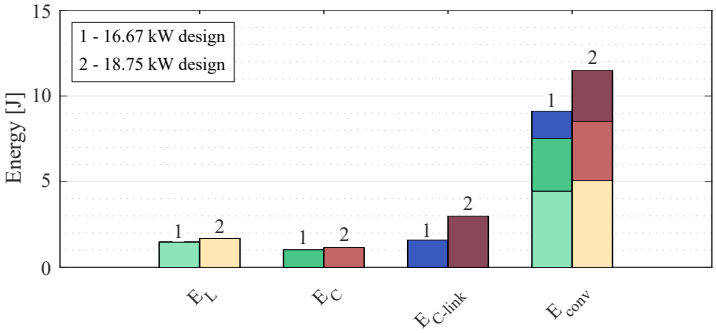


Figure 13. Comparison of the stored energy in the passive elements for $2L_C$ converter configurations.

4.3. Single-Stage with STATCOM Architecture-2L$_{st}$

Contrary to the $2L_C$ converters, whose consumed reactive powers were imposed by the capacitance value and the grid frequency, the reactive power handled by the STATCOM was adjusted to the one required by the active rectifier in $2L_{st}$ configuration. Hence, in terms of the $2L_{st}$ architecture, while the active rectifier focuses on transferring the SG active power to the 270 V_{DC} bus, the STATCOM was disconnected from the distribution bus and established its own DC-link voltage, as presented in the architecture schema of Figure 14. This way, the STATCOM worked as a variable capacitance for reactive power compensation throughout the SG grid frequency range. In addition, the identical design of both the active rectifier and STATCOM (passive elements, semiconductors, heat sink, etc.) allow designing an architecture with a higher redundancy degree, in case of a power converter failure. In fact, by means of the DC bus voltage control, a power converter could be connected to the DC distribution bus to transmit active power (rectifier operation) or be disconnected to establish its own higher DC bus voltage and compensate reactive power (STATCOM operation). Therefore, if each additional converter could operate as either a rectifier, which transfers active power, or as a STATCOM for reactive power compensation, functional redundancy is also supported.

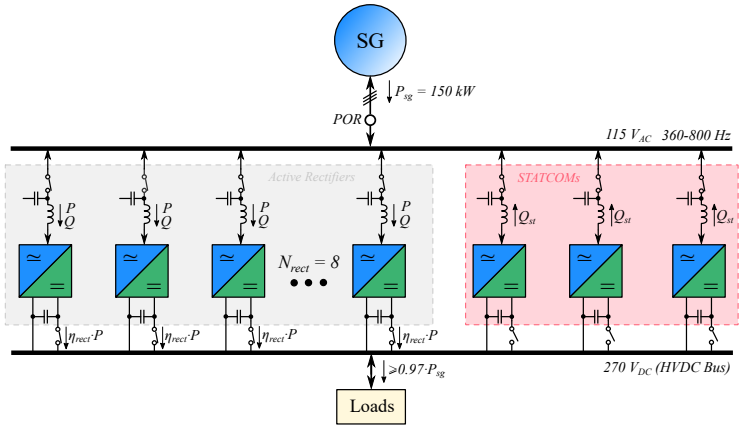


Figure 14. Simplified schema of the proposed active modular $2L_{st}$ architecture structure.

Regarding the design of the power converter, the operating PF of the active rectifier follows the maximum PF limit curve during the whole frequency range, as a consequence of the variable capacitance behaviour of the STATCOM (see Figure 5). Thus, designing the power converter for a single PF point might be a difficult task because the V_L value changes with f, resulting in a change on the required operating PF value for the active rectifier. The PF range depicted in the curve of Figure 5, though, describes the maximum average value of the PF points between V_L = [25.46, 56.58] V for the grid frequency range between 360 and 800 Hz. Hence, the active rectifier is designed to follow this operating PF range, which presents the maximum PF average value.

From the defined PF range, the maximum reactive power demand operating point is selected as the active rectifier design point (see Figure 5), i.e., $V_L = 25.46$ V and PF = 0.924. Hence, assuming $f = 360$ Hz, the design point data ($V_{ph} = 115$ V, $V_L = 25.46$ V and $\cos(\varphi) = 0.924$) and using (14), the converter input filter inductance, L, can be calculated depending on the converter nominal power, P. Consequently, the input filter capacitance, C, is designed for fulfilling DO-160G harmonic requirements. In addition, based on this design point, the operating PF of the active rectifier can be analyzed for the different input voltage conditions from where it is concluded that the worst case operating current, which occurs when $V_{ph} = 122$ V and $f = 360$ Hz, is 8.4% larger than the design point current.

As previously explained, even if the active rectifier and the STATCOM is the same converter, the STATCOM is disconnected from the 270 V distribution bus and, hence, it establishes its own DC bus voltage. Under the approach of the same maximum current for both rectifier and STATCOM operations, the DC bus voltage for the STATCOM is defined as 459 V using (13) and assuming $V_{ph} = 122$ V and $f = 800$ Hz. As the selected semiconductor is rated at 650 V blocking voltage, the difference between the semiconductor voltage rating and the STATCOM dc-link steady-state voltage is established in 1.42 times (≈ 1.5 times), being an acceptable limit for aviation applications [23].

From these design considerations, the thermal analysis was performed assuming the worst case operating condition for both the active rectifier and the STATCOM (see Figure 6). As expected, the STATCOM operation results were limited in defining the switching frequency of the converter due to the higher DC bus voltage and, hence, higher switching losses for the same maximum current. Since 100 kHz of switching frequency is desired for achieving a compact converter, the converter nominal power is defined to be 18.75 kW from the thermal analysis results. Consequently, eight active rectifiers are required in this architecture for transferring the 150 kW nominal power of the SG. The number of STATCOMs, N_{st}, though, is calculated as,

$$N_{st} = ceil\left(\frac{N_{rect} \cdot (P \cdot \tan(\varphi) - i_C)}{i_{L-max} + i_C}\right) \tag{20}$$

being N_{rect} the number of rectifiers, i_C the delivered reactive current by the input filter capacitors and, i_{L-max} the maximum current supplied by the STATCOM flowing through the input filter inductance, i.e., the worst case operating current previously mentioned. From (20), it is observed that by increasing the input filter capacitor, and thus, i_C: (a) the demanded reactive current to the STATCOM can be decreased according to the numerator; and, (b) the delivered maximum reactive current by a STATCOM can be increased according to the denominator. Hence, N_{st} can also be decreased by increasing C.

In this regard, Figure 15 presents the power losses defined by the $2L_{st}$ architecture at the worst nominal conditions ($V_{ph} = 115$ V and $f = 360$ Hz) depending on the input filter capacitance, where the first capacitance value represents the C required for harmonic fulfilment. Note that, increasing C, though, it also means increasing the overall architecture volume of the passive elements. In addition, reducing N_{st} results in a higher thermal stress per STATCOM due to the increased losses. Since the highest thermal stress is given in the STATCOM, the input filter capacitance is increased up to 19 µF while N_{st} is maintained to be 3 (see Figure 15). Thus, the design and electrothermal analysis results of the architecture are summarized in Table 3 and the "oversized" DM filtering results in Figure 16. Note that, aiming to squeeze the overfiltering effort, reduce the thermal stress, and increase the architecture efficiency, the switching frequency is decreased to 80 kHz.

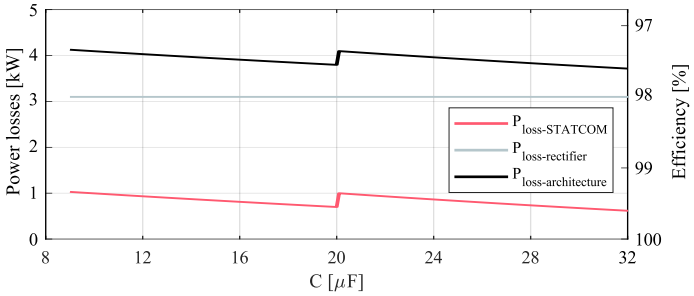


Figure 15. The $2L_{st}$ architecture efficiency depending on the input filter capacitance (operating at $V_{ph} = 115$ V and $f = 360$ Hz).

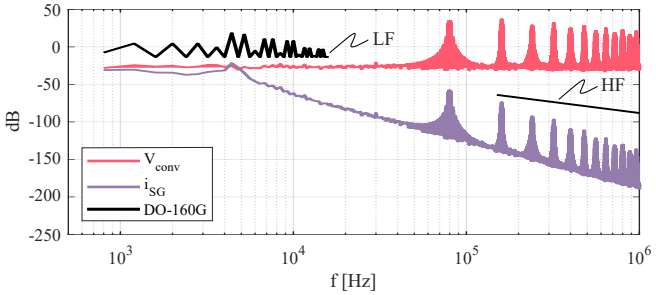


Figure 16. DM input filter results of $2L_{st}$ architecture for fulfilling LF and HF requirements.

5. Comparative Analysis among Different Architectures

Based on the presented $2L_2$, $2L_C$, and $2L_{st}$ architecture designs, this section provides an comparative analysis in order to decide the most suitable active modular architecture for the defined MEA application. Thus, following the evaluation parameters described in Section 3, the selected architectures are compared in Figure 17. Note that the presented results are normalized between 0 and 1 values for comparative purpose, where, for each compared parameter, the obtained maximum value is considered to be 1.

In terms of efficiency, almost no difference can be found among the three topologies when operating close to nominal power values. We should note that, when operating at relatively low power values (below half power), $2L_C$ and $2L_{st}$ architectures present efficiency below 97% due to the reactive power consumed. In the case of $2L_{st}$, though, STATCOM could be switched off to increase the architecture efficiency above 97%, owing to reactive power handling.

Regarding the design, $2L_C$ architecture is the most simple and cost-effective in terms of overall semiconductor number ($N_{conv} \cdot N_{dev}$). The stored energy in the passive elements and the expected lifetime, however, become the main drawbacks of this topology. The $2L_2$ architecture is beneficial, not only in this context but also in the reliability aspects. A low FIT/cm^2 is expected from this architecture and, advantageously, the largest lifetime can be expected according to the result of B_1. Nevertheless, operating with two DC/DC stages in parallel (per converter) increases the complexity of this architecture. Due to the higher thermal stress and blocking voltage of the STATCOM in $2L_{st}$ architecture, a lower reliability degree is expected from the overall architecture compared to the $2L_2$ architecture, especially in terms of FIT/cm^2. However, this issue could be improved by employing a higher voltage rating power device in the STATCOM and, hence, increase B_1 and λ parameters. A higher blocking voltage ratio will improve the reliability in terms of FIT/cm^2 and increase the STATCOM power device's current rating and, thus, reducing the thermal stress will increase the architecture lifetime. In addition, since the operating STATCOM could operate as active rectifiers, in case of power converter failure, three additional redundancies are provided by $2L_{st}$ architecture to ensure the nominal SG power distribution.

If a power converter of the $2L_{st}$ architecture failed, the grid PF would be diminished while the active power could be maintained at maximum. On the contrary, if a power converter failed in $2L_2$ and $2L_C$ architectures, the delivered active power would decrease.

Thus, in order to evaluate the influence of redundancies in the architecture volume, costs, and complexity, an additional normalized analysis is presented in Figure 18, focusing on the volume of the passive elements, the cooling system volume, and the number of power devices. As a result, the three additional redundancies in the $2L_C$ architecture is counterproductive in terms of the passive elements volume. Regarding complexity and costs, $2L_2$ architecture is the one hindered by an overall number of power devices, which almost doubles the required ones by the $2L_{st}$ architecture. In this context, $2L_{st}$ architecture is the most cost-effective architecture, while maintaining a relatively low volume when three redundancies are considered. Therefore, $2L_{st}$ architecture is considered the most suitable architecture for the defined application.

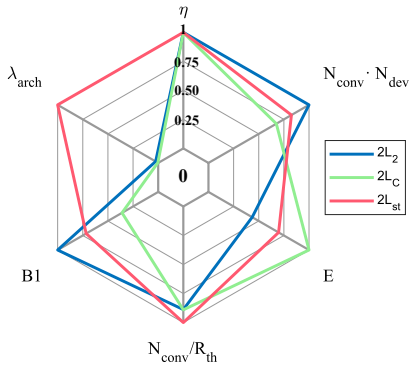


Figure 17. Normalized comparative analysis among the designed $2L_2$, $2L_C$, and $2L_{st}$ architectures.

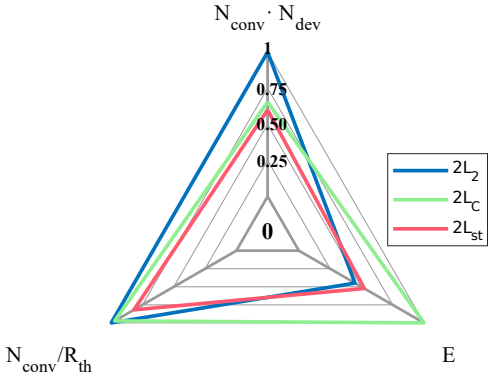


Figure 18. Normalized comparative analysis among $2L_2$, $2L_C$, and $2L_{st}$ architectures when three redundancies are considered.

6. Conclusions

The continuous development of aircraft electrification has led toward the research and development of innovative and reliable electric drive architectures. Considering the up-to-date 115 V_{AC} input and a 270 V_{DC} output rectification scenario, three active rectifier configurations were proposed to replace the traditional ATRU technology. However, identifying the most suitable configuration for implementing an active modular architecture is not a straightforward decision, due to the different attributes that surround each configuration. Thus, a comparison framework is proposed, which evaluates efficiency, reliability, and power density (referred to architecture volume), which are considered crucial parameters in aircraft applications.

The design criteria of $2L_2$, $2L_C$, and $2L_{st}$ architectures were presented and comparisons among the three architectures were performed. The three architectures are designed to fulfil the operating, power quality and harmonic requirements of aviation standards. Thus, the three architectures achieve an efficiency above 97% when operating at nominal conditions and a high power quality (referred to as THD_i below 1%). The $2L_C$ architecture is the

most simple, but also the most bulky in terms of stored energy. In addition, the fact of suffering from higher thermal stress makes this architecture less attractive than the other proposals in terms on wear-out failures. The $2L_2$ architecture, on the contrary, stands as the most compact architecture. Moreover, the highest reliability in terms of wear-out failures is achieved by this architecture. This fact is achieved by means of paralleling the DC/DC stage, which, inherently, is translated into an increased complexity. The $2L_{st}$ architecture presents potential results in terms of complexity and volume. However, the higher DC bus voltage and thermal stress of the STATCOM penalizes the architecture in terms of reliability, this issue could be solved by employing a higher voltage rating power device improving and, therefore, reliability parameters. In addition, the fact that the active rectifier and STATCOM are identical converters provides the architecture with a higher redundancy degree compared to the other proposals. In fact, a different paradigm is observed if three redundancies are considered in every architecture, which are already provided by $2L_st$ architecture.

The three additional redundancies emphasize the large volume related to the stored energy in $2L_C$ architecture. Additionally, a relatively large number of power devices is required for the $2L_2$ architecture (almost double the $2L_{st}$ architecture) which, indeed, can be translated to larger costs and complexity apart from assuming a parallel operation of the devices in the DC/DC stage. Consequently, the $2L_{st}$ architecture is preferred, not only because lower complexity and costs are expected, but because a relatively low volume is achieved, while providing high efficiency, high power quality, and a high redundancy degree.

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Appendix A. Starter-Generator Impedance Estimation

According to [57], the synchronous impedance, Z_{SG}, of the SG, can be estimated as,

$$Z_{SG} = 3 \cdot \frac{V_{ph}^2}{S} \tag{A1}$$

where V_{ph} corresponds to the nominal phase to neutral RMS voltage, and S to the machine apparent power deduced for a 0.8 PF. Assuming that the machine resistance is neglected for simplification purposes, the synchronous inductance, L_{SG}, is calculated as,

$$L_{SG} = \frac{Z_{SG}}{2\,\pi\,f} \tag{A2}$$

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