



## **Specialized EMI Shielding Process for Semiconductor Package**

**Rennier S. Rodriguez<sup>1\*</sup> and Frederick Ray I. Gomez<sup>1</sup>**

<sup>1</sup>*New Product Development and Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027 Philippines.*

### **Authors' contributions**

*This work was carried out in collaboration amongst the authors. Both authors read, reviewed and approved the final manuscript.*

### **Article Information**

DOI: 10.9734/JERR/2020/v19i417238

#### Editor(s):

(1) Dr. David Armando Contreras-Solorio, Autonomous University of Zacatecas, Mexico.

#### Reviewers:

(1) Alemu Gurmessa Gindaba, Wollega University (WU), Ethiopia.

(2) Asmaa Shawqy Khaleel, Baghdad University, Iraq.

Complete Peer review History: <http://www.sdiarticle4.com/review-history/63531>

**Original Research Article**

**Received 02 October 2020**  
**Accepted 08 December 2020**  
**Published 19 December 2020**

### **ABSTRACT**

Electromagnetic interference (EMI) is an unwanted disturbance caused by external sources that would affect the electrical functionality of the device. This paper presents an advanced approach of electromagnetic interference (EMI) shielding protection for sensitive and critical semiconductor packages. The process employed half-cutting method to apply the EMI coating on the upper-half portion of the device, protecting the Silicon die and internal components from external EMI disturbance. Eventually, the enhanced EMI shielding process would provide advantages of improved quality and eliminate risks of possible assembly issues while providing the main purpose of EMI protection for semiconductor devices. For future studies, the technique could be applied on packages with similar requirement. Prototypes are helpful to validate the effectiveness of the enhanced process.

**Keywords:** *Assembly process; EMI; EMI shielding; half-cut; lamination; semiconductor.*

\*Corresponding author: Email: [rennier.rodriquez@st.com](mailto:rennier.rodriquez@st.com);

## 1. INTRODUCTION

Electromagnetic interference (EMI) may be inevitable, but techniques exist to shield or protect the semiconductor integrated circuit (IC) from this disturbance. Semiconductor manufacturing companies are continuously enhancing and developing methods and techniques for EMI shielding such as integrating metal cans and board-level shielding that is coupled to the grounding connection of the system. Conductive metal envelops the EMI-prone area in a system as shown in Fig. 1.

Some semiconductor companies have technologies to provide external EMI coating through system called spray painting and

sputtering method as shown in Fig. 2, with such EMI shielding solutions adapted by other companies giving them alternative process for solving the issues on EMI. Fig. 2 shows a typical semiconductor device with EMI shielding, and Fig. 3 shares the alternative EMI shielding process.

EMI solution to packages comes with different approach on how the problem would be dealt. During evaluation and validation, different concerns and issues are highlighted: 1) indirect material such jig will be subjected to disposal after usage, 2) parts of the units that should not be coated are contaminated during coating, and 3) difficulty to control the thickness of the coating material.

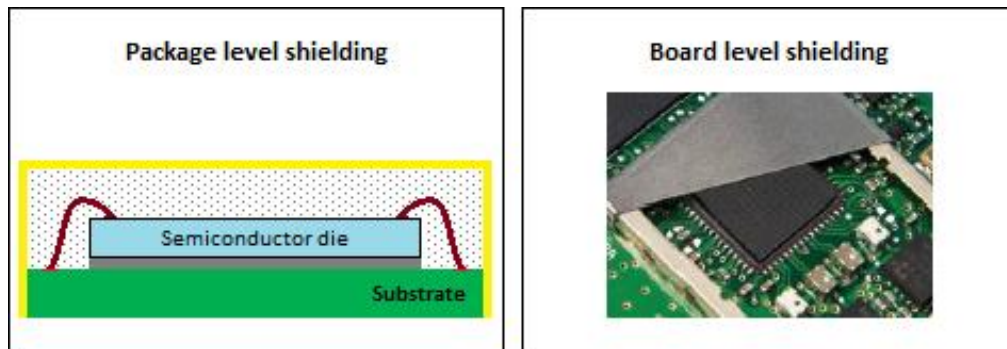


Fig. 1. EMI shielding techniques

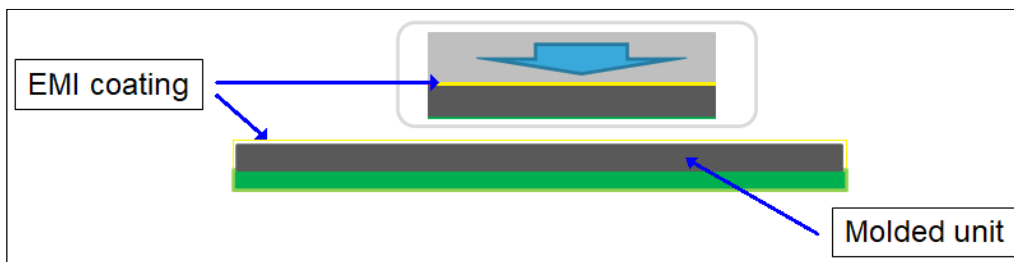


Fig. 2. EMI shielding representation

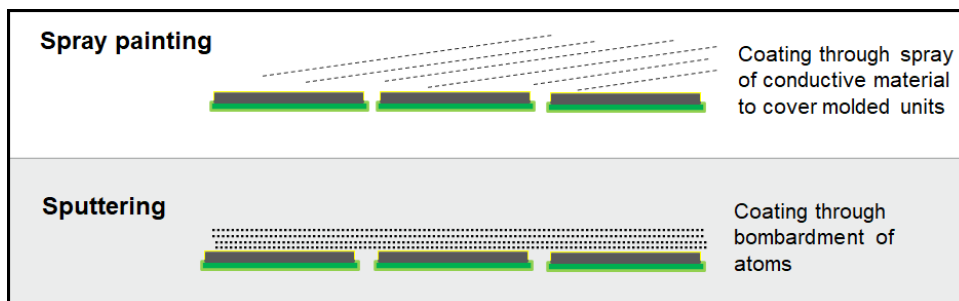


Fig. 3. Other EMI shielding techniques

## 2. METHOD AND RESULTS

The specialized EMI shielding process follows the improved assembly process flow shown in Fig. 4 modified to integrate the half-cutting the molded units according to required package size of the product. Worthy to note that assembly manufacturing process flow differs with the technology, the product, and/or the application [1-4]. With continuing technology development and breakthroughs, challenges in assembly manufacturing are inevitable [5-7]. Highlighted in the shown process flow are the integrated process steps necessary for the specialized EMI shielding.

Half-cut singulation process shown in Fig. 5 prepares the units for application of EMI coating on the upper-half portion of the device. EMI coating through lamination of conductive film material into the units using lamination machine is illustrated in Fig. 6. The application of heat during lamination would transform the conductive film into gel-like material covering the upper-half portion of the molded units.

Full-cut singulation process is eventually done to singulate or cut into individual units according to package requirement. Fig. 7 shows the singulated unit.

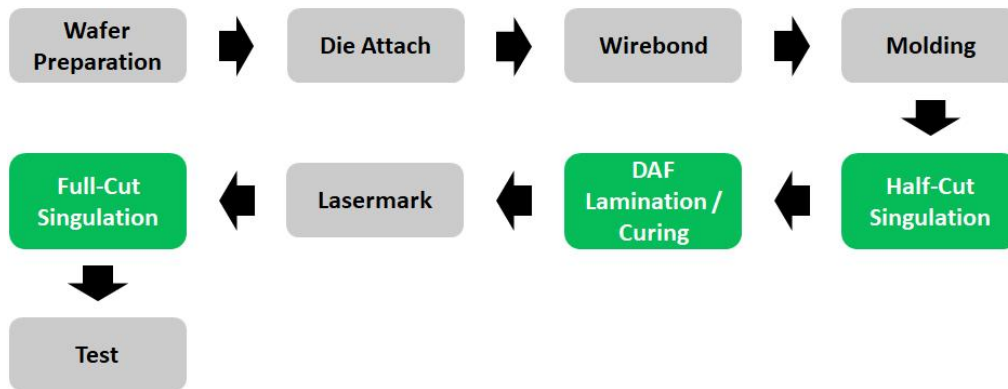


Fig. 4. Assembly process flow for new EMI shielding

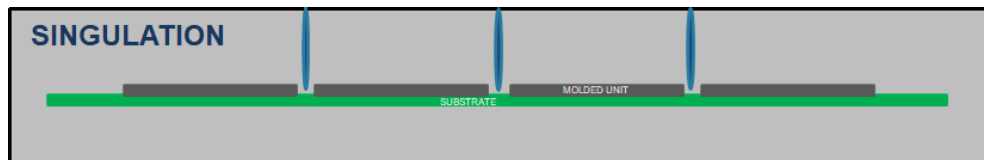


Fig. 5. Half-cut singulation process



Fig. 6. Lamination process



Fig. 7. Singulated unit with EMI shielding

### 3. CONCLUSION AND RECOMMENDATIONS

The specialized EMI shielding process presented in this paper provides an alternative solution for EMI protection on critical semiconductor devices. The enhanced process would also contribute to improved quality of the product and the assembly process and would eliminate risks of possible assembly issues such material scrappage during process, contamination during coating, and difficulty to control the thickness of the coating material.

Semiconductor devices with similar case could use the technique for EMI shielding process. Further discussion of the design and process in this paper is available in [8]. Though the paper is focused on the EMI shielding ability, continuous process and design improvement is essential to foster and sustain high quality performance of semiconductor products and its assembly manufacturing. Prototypes are helpful for future works to validate the effectiveness of the enhanced process. With EMI and electrostatic discharge (ESD) sharing common characteristics, it is imperative that the fabrication method and all other assembly processes observe proper ESD checks and controls. Works and learnings discussed in [9-11] are helpful to achieve proper and effective ESD-related controls.

#### DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

#### ACKNOWLEDGEMENT

The authors would like to express gratitude to the New Product Development & Introduction (NPD-I) team and the Management Team for the continuous support.

### COMPETING INTERESTS

Authors have declared that no competing interests exist.

### REFERENCES

1. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
2. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008;1-11.
3. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
4. Tsukada Y, et al. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
5. Nenni D, McLellan P. Fables: the transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
6. Coombs C, Holden H. Printed circuits handbook. 7th ed, McGraw-Hill Education, USA; 2016.
7. Harper C. Electronic packaging and interconnection handbook. 4th ed, McGraw-Hill Education, USA; 2004.
8. Rodriguez R, et al. Method for making a shielded integrated circuit package with an electrically conductive polymer layer. US patent no. 9761538; 2017.
9. ESD Association. Fundamentals of ESD, device sensitivity and testing. USA; 2011.
10. Gomez FR, Mangaoang Jr. T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.
11. Gomez FR, et al. Protection from ESD during the manufacturing process of semiconductor chips. US patent no. US10388594; 2019.

© 2020 Rodriguez and Gomez; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (<http://creativecommons.org/licenses/by/4.0>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:

The peer review history for this paper can be accessed here:  
<http://www.sdiarticle4.com/review-history/63531>