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Silicon Die with Integrated Epoxy for Improved Interface Adhesion

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Authors' contributions

This work was carried out in collaboration between the authors. Both authors read, reviewed, edited, and approved the final manuscript.

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ABSTRACT

Breakthroughs and innovations are constantly being developed in electronic packaging industry to address the manufacturing challenges and overcome existing assembly limitations. An augmented design of thin Silicon die is introduced to establish a robust and improved interface adhesion between the die and the die attach material during the die attach process. The wafer preparation flow is also presented. The realization of the augmented die design with integrated epoxy material would ultimately provide a robust connection and would mitigate the die attach related issues such delamination, die cracks and voids.

Keywords: Adhesion; delamination; die attach process; glue; epoxy; silicon die.

1. INTRODUCTION

Wafer preparation and die attach processes have assembly manufacturing challenges especially in handling or processing thin Silicon dies with thickness of 70 µm (micron) to 130 µm. Potential Silicon die-related issues such as the die delamination, die cracks, and die attach epoxy voids occur specifically on thin die applications during the die attach process. An image in Fig.1. captured using scanning electron microscope (SEM) shows the cross-sectional view of a

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delamination between the die and the glue die attach material.

Die delamination in an electronic device is the separation of the die attach material to the Silicon die. A small delamination when aggravated may worsen and propagate resulting to a complete delamination of the die to the glue. Delamination may also propagate to other interfaces inside the quad-flat no-leads (QFN) package, for instance the die-to-carrier, mold-to-die or mold-to-carrier interfaces. With the growing demand on thin die applications, elimination of die and die attach related issues is one significant challenge during wafer preparation and the die attach process.

2. DESIGN SOLUTION

The formation of the glue fillet height on the sidewall of the die is a normal response of the glue or epoxy when a die is attached. A new Silicon die design with integrated epoxy shared in Fig. 2. would provide a natural adhesion to the succeeding glue or epoxy material during the die attach process.
Silicon die bottom side backside area is augmented with the pre-applied epoxy die attach material on the grooved periphery. With the integrated epoxy material, the die attach coverage is enhanced and the die attach adhesion is reinforced and becomes more robust. The new die design offers a potential solution to eliminate the delamination formed between the interface of the die and die attach material during the die attach process. Fig. 3. illustrates the updated wafer preparation flow to reflect the added steps specific for the new die design with integrated epoxy material. Laser grooving technology is used in the formation of the peripheral groove.

As earlier mentioned, the augmented die design with integrated epoxy material could help mitigate die to die attach delamination. Lower coefficient of thermal expansion (CTE) mismatch is also created between the pre-applied epoxy material and the subsequent die attach material. Fig. 4. shows the cross-sectional representation of a QFN leadframe device using the new Silicon die design with integrated epoxy material, highlighting the adhesion interface between the two die attach materials. Furthermore, die cracks could be prevented and die attach voids could be minimized with the application of the new design.

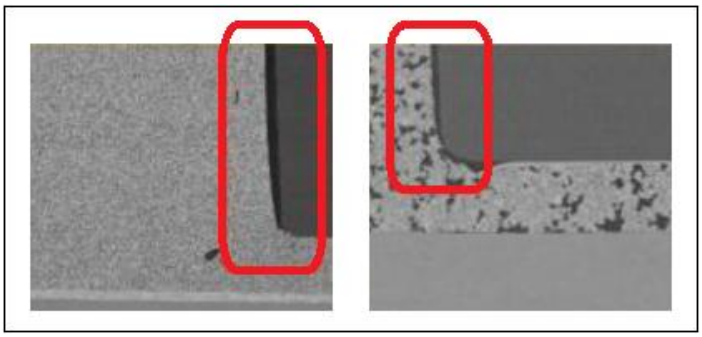

Fig. 1. SEM photo of silicon die interface with glue

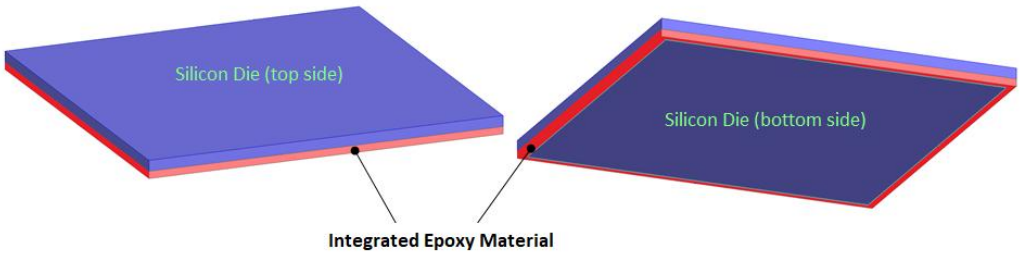

Fig. 2. Silicon die with integrated epoxy 3D view

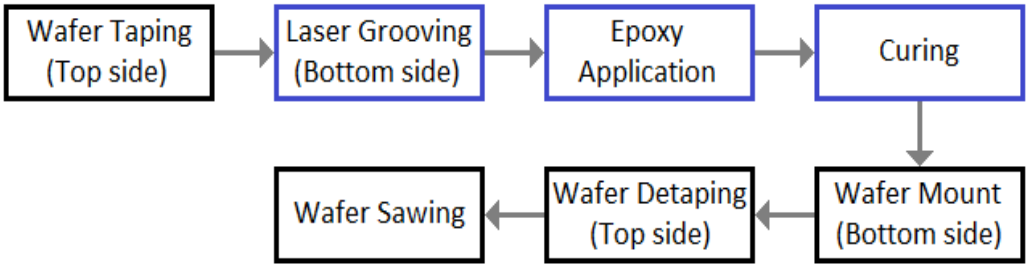

Fig. 3. Wafer preparation flow

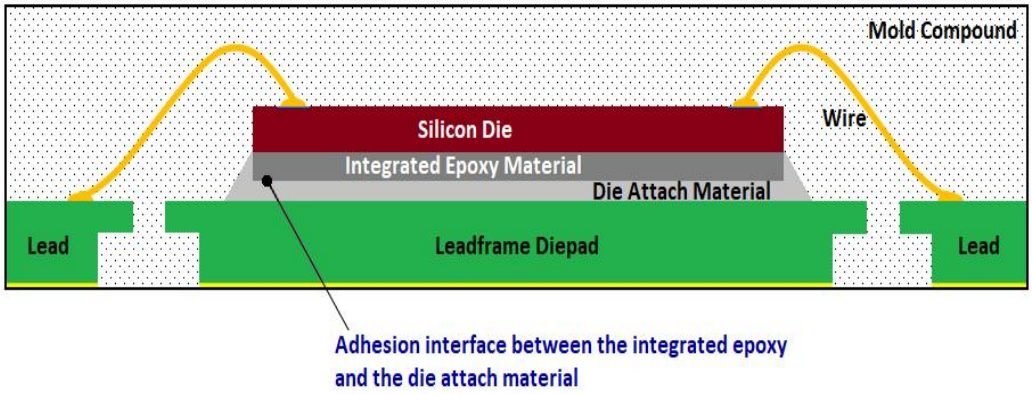

Fig. 4. Cross-sectional view of the QFN package

3. CONCLUSION

The paper presented a new Silicon die design with integrated epoxy die attach material for establishing a robust interface with the subsequent die attach material. With the improved design, die attach delamination issues as well as die cracks and die attach voids could eventually be mitigated. Future works could use the new die design to realize a robust die attach process and prevent any die attach related assembly issues. For references, works shared in [1-5] are helpful in tackling delamination issues. Studies and learnings discussed in [6-12] are useful to address other die attach related challenges.

DISCLAIMER

The company name used for this research is commonly and predominantly selected in our area of research and country. There is absolutely no conflict of interest between the authors and company because we do not intend to use this company as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the company rather it was funded by personal efforts of the authors.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Pflügler N, et al. Temperature-dependent adhesion measurements of die attach materials to moulding compounds and lead frame surfaces enabling robust package designs. 7th Electronic System-Integration Technology Conference (ESTC); 2018.
2. Buenviaje Jr. S, et al. Process optimization study on leadframe surface enhancements for delamination mitigation. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;95-100.
3. Alberici S, et al. Organic contamination study for adhesion enhancement between final passivation surface and packaging molding compound. Microelectronic Engineering. 2004;76(1-4);227-234.

4. Gomez FR, Seguido R. Improvement on semiconductor substrate design with package modeling and simulation for mitigation of delamination and voids. Journal of Engineering Research and Reports. 2018;2(4):1-9.
5. Teng WH, Wei HC. An analysis on oxidation, contamination, adhesion, mechanical stress and electro-etching effect toward dip package delamination. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT); 2010.
6. Chang M, Li A. Low stress die attach material challenges for critical Si node with Cu wire. 16th IEEE Electronics Packaging Technology Conference (EPTC); 2014.
7. Manikam VR, Cheong KY. Die attach materials for high temperature applications: a review. IEEE Transactions on Components, Packaging and Manufacturing Technology. 2011;1(4);457-478.
8. Zhang R, et al. Solutions for controlling resin bleed out. Solid State Technology. 2017;60(9);16-19.
9. Graycochea Jr. E, et al. Process enhancement to eliminate adhesive film remains during die picking. Journal of Engineering Research and Reports. 2020;11(3);1-4.
10. Xian TS and Nanthakumar P. Dicing die attach challenges at multi die stack packages. 2012 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.
11. Neff B, et al. No bleed die attach adhesives. IEEE International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces. USA. 2005;1-3.
12. Hsiung JC, et al. A surface energy approach for analyzing die attach adhesive resin bleed. Journal of Adhesion Science and Technology. 2003;17(1);1-13.

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