LOW POWER CIRCUIT FOR BRENT-KUNG ADDER BASED ON ADIABATIC LOGIC

Dhasarathan S,
Department of Electronics and Communication Engineering,
PR Engineering College,
Thanjavur, India
dhasarathan.raja@gmail.com

Abstract: Adiabatic logic circuit designs are used to reduce power dissipation in any circuits. For low power and low noise emission applications, adder plays a vital role. The Complementary Metal Oxide Semiconductor (CMOS) design of 16-bit Brent-kung adder provides less number of gates but it generates high power due to switching activities of the design. To overcome this problem, 16-bit Brent-kung adder is designed using complementary Pass Transistor Energy Recovery adiabatic Logic (CPERL) with less number of gates. Also, low power dissipation is achieved which can be used for long life battery operations. The CPERL based system offers 59.97% reduction in power when compared to the conventional design. Experimental results are obtained using TANNER EDA tool 13.1.

Keywords: CMOS, Brent-kung adder, adiabatic logic, Tanner EDA.

I. INTRODUCTION

The adiabatic logic circuits are used to save power during switching activities. Adiabatic logic using Split level Charge Recovery Logic (SCRL) and two Level Adiabatic Logic (2LAL) is described in [1].The SCRL is similar to the NAND and the major difference is instead of Vdd and Gnd in NAND, SCRL uses the trapezoidal clocks $\Phi 1$ and $\Phi 2$. Two designs for SRAM using 2LAL is described in [2]. To design the RAM only transmission gates are used with zero CMOS inverters for cross coupling. A comparison of the adiabatic logic methodologies with CMOS design is described in [3]. The results proved that adiabatic logic provides less power dissipation than CMOS design.

The adiabatic logic for universal gates, decoder, multiplexer, D-flipflop and inverter is designed in [4] and it compares the average power with the conventional method. A fully adiabatic pipelined logic for MEMS resonators using 2LAL is described in [5]. To enhance the effectiveness of area efficiency and Q factor, resonator design is optimized. Carry Look Ahead (CLA) adder using CPERL is described in [6]. By utilizing the bootstrapping approach the high power dissipation and non-adiabatic loss in charge steering are eliminated. Full adder using Positive Feedback Adiabatic logic (PFAL) and Efficient Charge Recovery Logic (ECRL) is described in [7]. By using such logic approaches the energy is conserved with less heat dissipation. CMOS based positive feedback amplifier is described in [8] which is based on the dual rail logic. To operate such cascaded gate it requires three power lines.

Clocked adiabatic logic is described in [9]. From the DC power supply, clocked adiabatic logic is operated on the basis of non-energy recovery mode. Two phase drive adiabatic dynamic CMOS logic is described in [10]. It utilizes two complementary sinusoidal power supply clocks and the structure is derived from the static CMOS logic. Three logic families such as 2N-2N2p logic, positive

feedback adiabatic logic and efficient charge recovery logic are described in [11]. They are compared in terms of their operating frequency and energy saving ranges.

A building of cascaded logic circuits is described in [12]. The discharging and charging control of the capacitive load is achieved by the input signal with a single time varying supply. Low power gates using reversible logic is described in [13]. It ignores the gates garbage output. Also, the performance is compared with different adders. Reversible energy recovery logic is described in [14]. An eight phase clocking approach is utilized for reversible logic based on dual rail adiabatic circuit. FinFET design using adiabatic logic is described in [15]. A test circuit for 8-state clock chain is also demonstrated.

In this study, 16-bit Brent-kung adder is designed using CPERL. The paper is organized into 4 sections. Section 2 describes the Brent-kung adder using CPER logic and section 3 describes the results and discussion. Section 4 describes the conclusion of the study for the design of Brent-kung adder using CPERL for 16-bit addition.

II. METHODS AND MATERIALS

Brent-Kung adder is the parallel prefix adder which has three stages; preprocessing, carry generation stages and sum bits. When comparing to other parallel prefix adder the Brent-kung adder requires less connecting modules and easy to built. Figure 1 shows the Brent-kung adder structure for 16-bit addition.

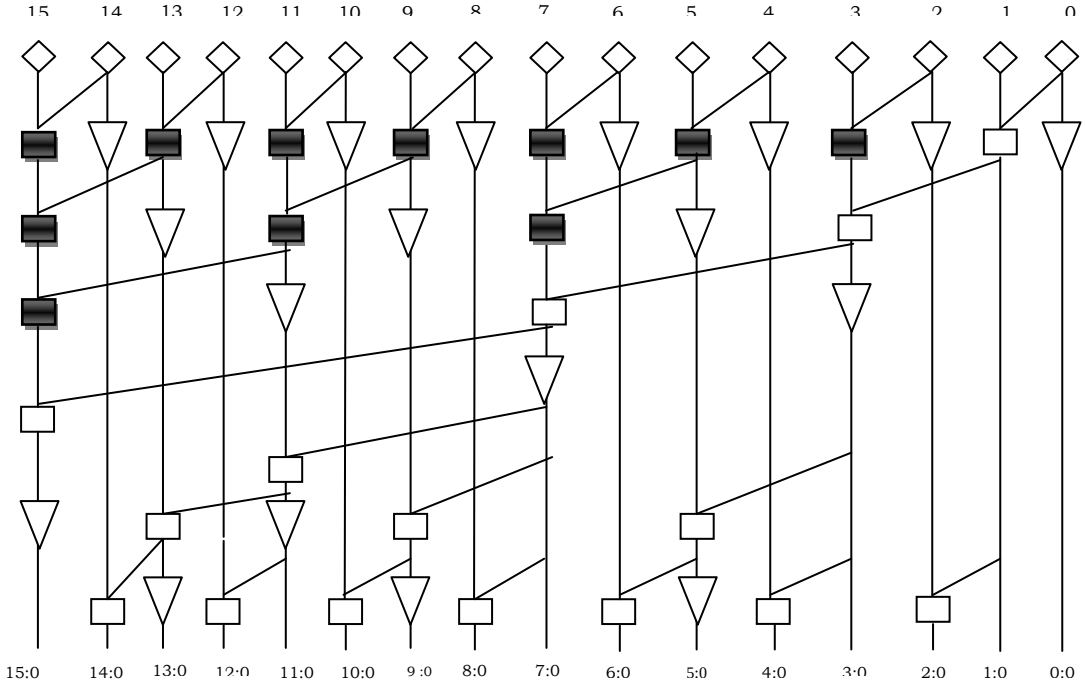
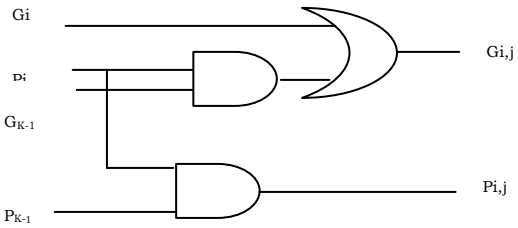


Fig. 1 Brent-kung adder structure for 16-bit addition

In order to obtain the carry bit signal, the signal will proceed from the preprocessing stage to carry generation stage. It has $2(\log N - 1)$ stages and avoids the explosion of wires. The carry generate part is represented as $G_{i,j} = G_{i,k} + P_{i,k} * G_{k-1}$ and propagate part is represented as $P_{i,j} = P_{i,k} + P_{k-1,j}$. The

adder stage is made up of two basic logic cells namely black cell and white cell. Figure 2 shows the black cell and white logic cell design.



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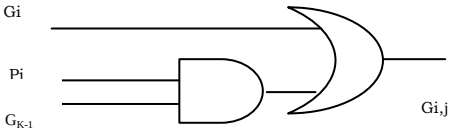
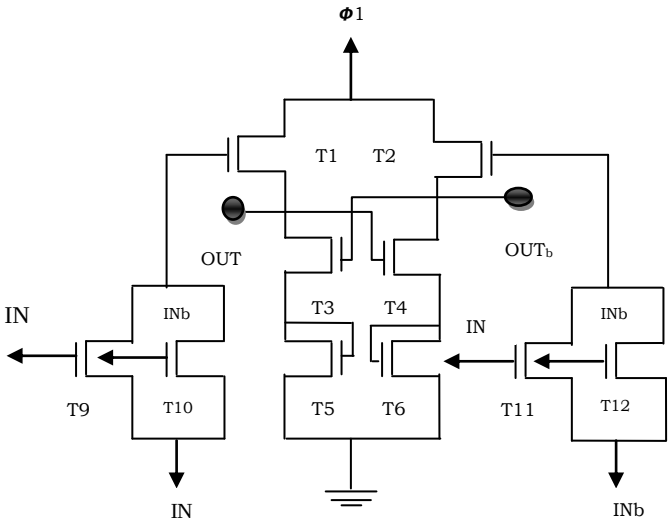


(b)

Fig. 2 Logic cells a) black cell b) white cell

The white cell calculates $G_{i,j}$ and black cell calculates both $P_{i,j}$ and $G_{i,j}$ and in the second stage the carry bits are generated and given to the third stage from the equation $Sum = P_i \; XOR \, C_{i-1}$. To design such adder using adiabatic logic in CEPRL, dual rail logic is used with diode free family. It requires only one phase power clock for the single CEPERL which is made up of two elements such as charge-discharge function and logic function. Without any specific latch, a pipeline structure can be realized directly. CPERL is a fully adiabatic logic which dissipates less energy. Figure 3 shows the CPERL structure and charge and discharge of PG. More information about CPERL structure can be found in [6].



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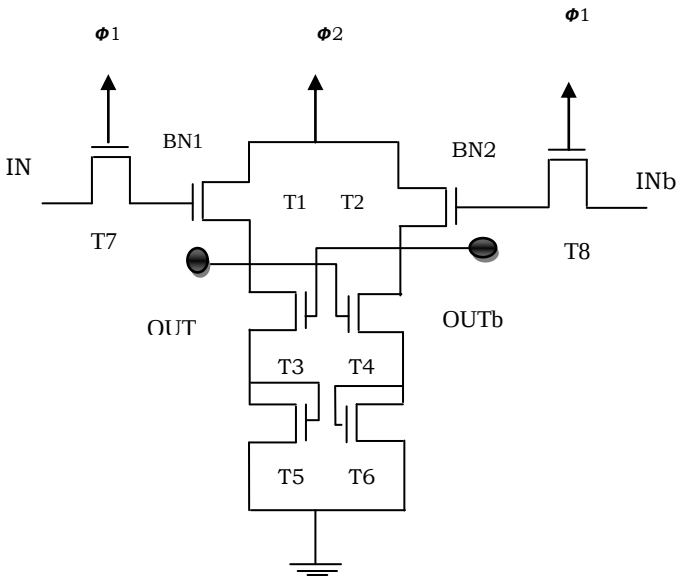
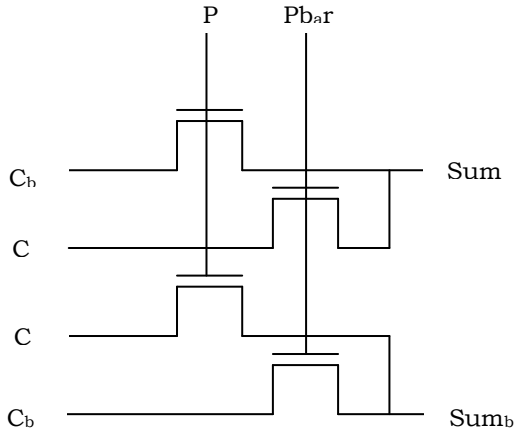


(b)

Fig. 3 a) CPERL inverter structure b) Charge- discharge of PG

Here ***Φ***1 and ***Φ***2 is the power clock supplies. For instance ***Φ***1 and IN are in same phase, If ***Φ***1 ramps up IN rises then INb remains low transistor T9 and T11 is ON BN1 is pre-charged to vdd to threshold (Vth) but BN2 is still at low voltage. If ***Φ***1 ramps down then IN also down and causes T9 and T11 OFF. Similarly ***Φ***2 is ramps up and due to the gate to channel capacitance in T1, BN1 goes to higher than Vdd by making T1 ON. ***Φ***2 charges the node OUT to V_{dd} in an adiabatic manner. when ***Φ***2 ramps down then the OUT goes down then charges stored on the OUT is recovered through discharge process. Where the transistor T1-T6 is the charge discharge element and T9-T12 is the logic function element. Figure 4 shows the sum unit, Propagate and Generate unit using CPERL logic for Brent kung adder.



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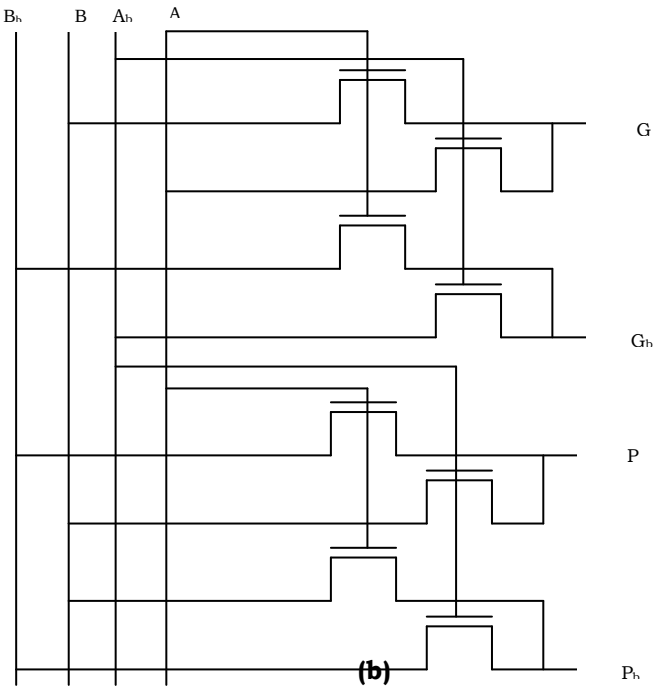

Fig. 4 CPERL logic for a) sum unit b) Propagate and generate unit

The sum unit and propagate generate unit using CPERL logic gates in the design of Brent-kung adder. Also, the amount of clock lines by the power-clock supply generator is minimized.

III. RESULTS AND DISCUSSION

The 16-bit Brent-kung adder using CPERL is simulated using TSPICE in Tanner EDA tool. The schematic structure is drawn in the S-EDIT and simulated in T-SPICE. The inputs A0-A15 values and B0-B15 values are assigned randomly. Figure 5 shows the simulation waveform of low power circuit using Brent-kung adder for the output sum.

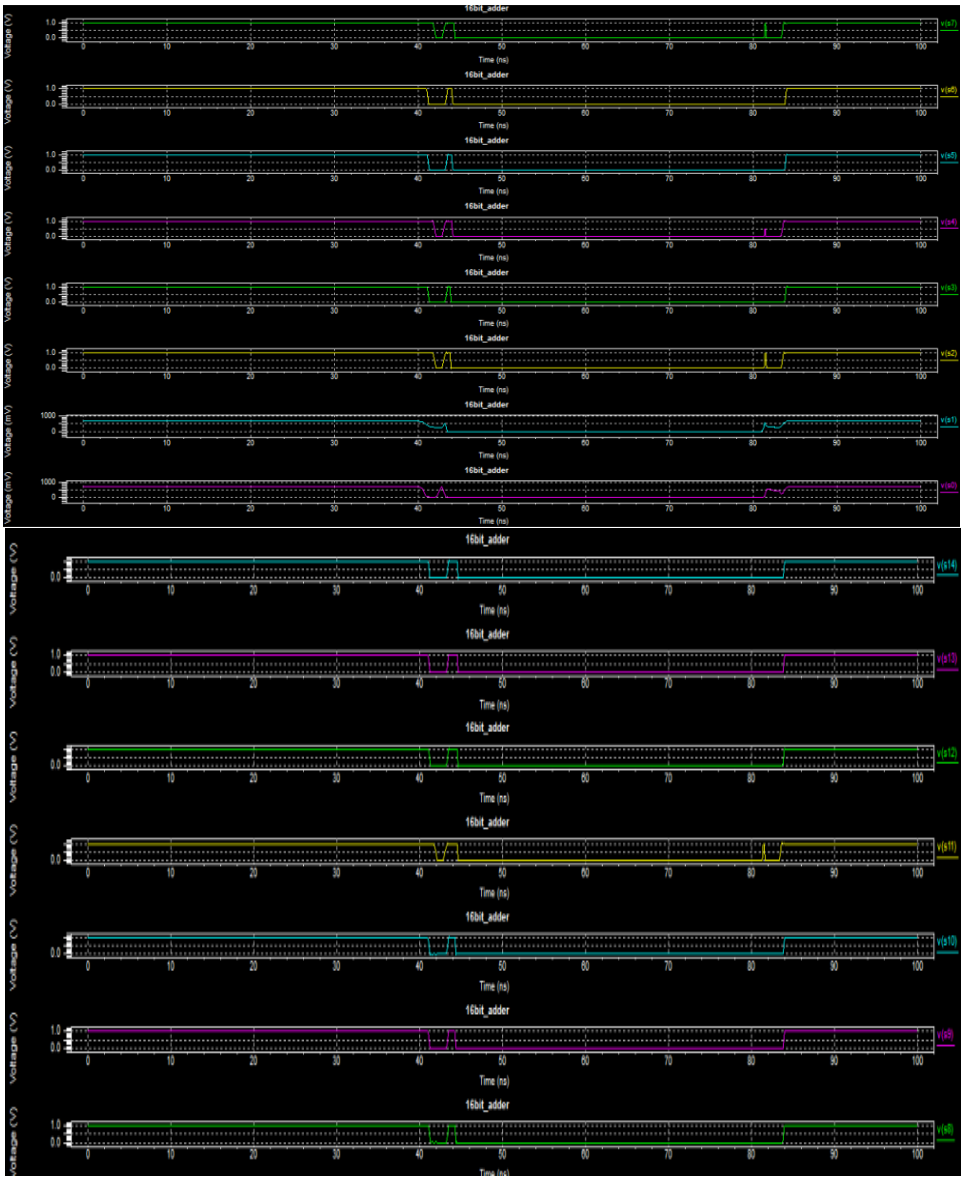

Fig. 5 Simulation of low power circuit using Brent-kung adder - output Sum (S0-S16)

For the given input A, B values, the Brent-kung adder using CPERL outputs the sum and carry bit. For instance If A0 is 0 (00000000 00000000) and B0 is 1(00000000 00000001) then the sum is 1(00000000 00000001). Figure 6 shows the performance analysis of the proposed method and conventional CMOS design in terms of power dissipation.

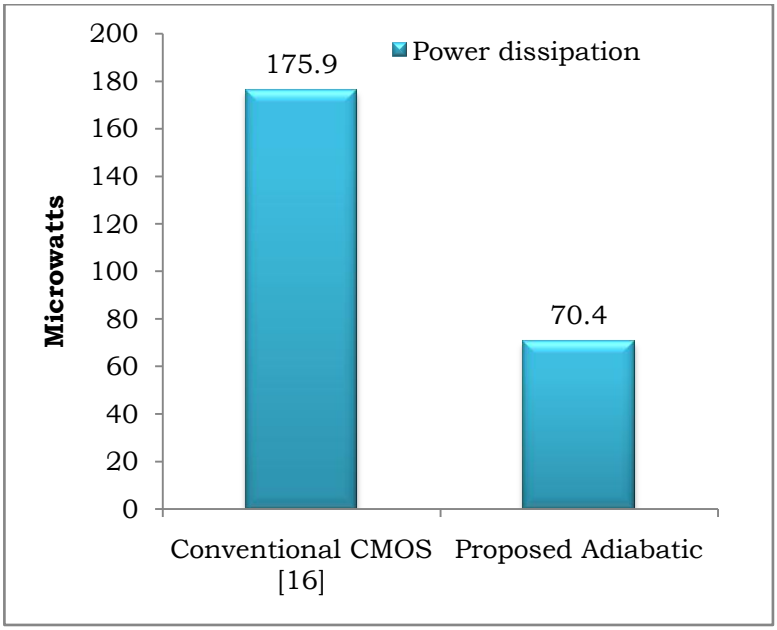

Fig. 6 Performance analyses of the Conventional CMOS and proposed method

It is observed that the power dissipation of the conventional method is 175.9μw where as it is 70.4 μw for 16-bit Brent-kung adder using CPERL. When compared to the conventional method for different inputs, the CPERL design provides good performance with more than 50% less power dissipation.

IV. CONCLUSION

In this study, a low power circuit for Brent-kung adder based on fully adiabatic logic is presented using CPERL approach. The circuit design is implemented in tanner EDA 13.1 tool. The comparison of the system with conventional method shows that the system offers more than 50% less power dissipation without degrading the output performances. This design can be used for long life battery functions. Also, the 16-bit Brent-kung adder using CPERL minimizes the non adiabatic energy loss dissipation by reducing the unwanted switching activities. In future, this study is extended to achieve less area using source coupled adiabatic logic with sinusoidal clock generator circuits using CPERL.

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