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Fabrication and electrical characterization of partially metallized vias fabricated by inkjet

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Abstract

Through silicon vias (TSVs), acting as vertical interconnections, play an important role in micro-electro-mechanical systems (MEMS) 3D wafer level packaging. Today, taking advantage of nanoparticle inks, inkjet technologies as local filling methods could be used to plate the inside the vias with a conductive material, rather than using a current method, such as chemical vapor deposition or electrolytic growth. This could decrease the processing time, cost and waste material produced. In this work, we have fabricated and demonstrated electrical characterization of TSVs with a top diameter of 85 μm, and partially metallized on their inside walls using silver nanoparticle ink and drop-on-demand inkjet printing. Electrical measurement showed that the resistance of a single via with a void free coverage from top to bottom could be less than 4 Ω, which is still acceptable for MEMS applications.

Keywords: TSV, inkjet, printed electronics, microelectronics packaging

(Some figures may appear in colour only in the online journal)

1. Introduction

Microelectronic devices are always going to be smaller, lighter, and more power efficient according to consumer demands. Therefore, 3D packaging technologies are a must to fabricate devices as small as possible. One of the key elements in 3D integration are the vertical interconnects between the stacked chips. An alternative way of making this interconnection is using conductive wirebonds just on the periphery of the chips [1]. A better alternative is using via holes through the silicon wafer/dies, called through silicon via (TSV). Using TSVs has several advantages over wirebonds. In this method, a high density of vertical interconnects are fabricated (not limited to the edge) on several thin chips stacked on top of each other with microbumps in between; This decreases the volume of device and since the vias are short, data transfer is faster with lower power consumption.

In order to have conductive interconnects, TSVs need to be metallized/filled partially or completely with a conductive material. In completely filled vias, stress caused by thermal expansion and thermal mismatch between metals and silicon is problematic; this could be minimized by not completely filling the vias. So in the case of partial metallization for some applications, the cost of ownership will be decreased because there are fewer reliability and yield issues [2]. For example, in case of Au or Cu metallization for RF applications, it is not necessary to completely fill the vias because the skin depth of these materials for RF signals in the GHz range is in μm range [2]. Currently, techniques like chemical vapor deposition (CVD) and physical vapor deposition (PVD) are used for the deposition of a seed layer inside the vias before deposition of the filling material like copper by electrochemical deposition (ECD), or electroplating to fill the vias completely [3, 4]. This kind of wet fabrication process is time consuming, expensive and not environmental friendly from the manufacturing point of view. Additive manufacturing such as inkjet printing could be a game changer in solving these problems.

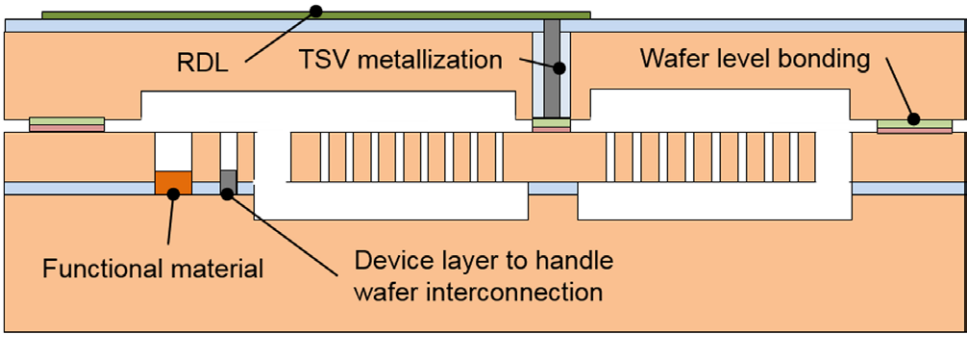

Figure 1. Selected steps in MEMS wafer level packaging with the potential to be fabricated by additive method.

TSVs also play an important role in wafer-level packaging of microelectromechanical systems or MEMS devices. Inkjet printing as an additive digital fabrication technique has the potential to be used to partially or completely metallize the via interconnects, instead of conventional electrodeposition (introduced in the PROMINENT consortium [5]), as well as for other selected steps in MEMS wafer-level packaging (figure 1) for instance redistribution layers (RDL) [6], which is not within the scope of this work. With this method, conductive material/ink is jetted just over the via holes without masking or removal of excess material that is done after the plating. Thus, the number of process steps and the amount of chemicals required could be reduced significantly, which makes the process more flexible, cost efficient and environmental friendly.

Previously, inkjet printing was used to metallize or fill the vias partially [7–9] or completely [10, 11]. The drop-size defines the minimum via diameter that can be filled by inkjet. The diameter of the droplet in air must be smaller than the diameter of the via. Currently, most of the printheads used in printed electronics are in order of 10 pl, and a 10 pl droplet has a diameter of 27 μm. Metallization of high density vias with a top diameter smaller than the drop dimeter of conventional inkjet printers was investigated in [12] using super inkjet (SIJ) with 0.1 femtoliter droplets. In [7] silver ink made of particles with mean diameter of 300 nm was used to realize the most optimum approach for having a homogeneous coverage on the side wall of the vias after the suitable sintering process. It was also claimed that partial coating of via walls is preferable because of the possible cracks in the vias that may be problematic in completely filled vias. In [8] we used silver nanoparticle ink to just coat the vias, and understand the effect of delay time between printed layers and substrate temperature on thickness, quality and uniformity of the wall coverage. In addition [9] investigated the fabrication of RDL and TSVs using a combination of inkjet and flexo printing. In this work, partially metallized TSVs are fabricated using inkjet printing and then electrically characterized. Via holes are fabricated on silicon wafer with plasma etching.

2. Materials and equipment

2.1. Materials

In this work, tapered shape TSVs are fabricated on silicon wafer with a top diameter of 85 μm, bottom diameter of 61 μm and depth of 116 μm, provided by Okmetic Inc. Vias were fabricated in five steps: (1) lithography (photoresist etch mask deposition and patterning), (2) plasma etching of the tapered vias, (3) photoresist mask removal, (4) thermal oxidation and oxide etch to reduce the roughness of the via sidewalls and (5) growing oxide layer for electrical insulation.

Table 1. Specifications of the NPS-J silver ink from Harima.

Particle size	8–15 nm (mean dia.12 nm)
Metal contents	62–67 wt%
Viscosity	7–11 mPa · s
Specific gravity	1.8–2.2
Solvent	Tetradecane
Curing conditions	220 °C (60 min)
Specific resistance	3 $\mu\Omega \cdot$ cm
Shrinkage	80–85%

Metallization of the vias' holes and also top and bottom routing were made with inkjet printing using silver nanopaste NPS-J from Harima Chemicals. Table 1 shows the reported specifications of the ink [13].

2.2. Fabrication equipment

A commercial drop-on-demand Dimatix Material Printer (DMP-2800) loaded with 10 pl cartridge was used to jet the nanometal ink into the via holes and also for patterning the conductive routes and pads on top and bottom layers.

The PM5 lapping and polishing machine from Logitech was used for thinning of the chips. More information regarding the silicon thinning can be found in [14].

2.3. Sample preparation and analyzation tools

A MicroAce Series 3 dicing saw from Leadpoit Limited was used to prepare the chips and the cross-sections of the metallized vias. A Zeiss Ultra 55 scanning electron microscope (SEM) and Olympus BX51 optical microscope were used to study the cross-section of the both blind and thinned vias. A Keithley 2400 sourcemeter attached to a probe station was used for electrical characterization.

3. Fabrication process

The fabrication process includes six steps (as shown in figure 2): (a) via-hole fabrication on silicon (process described

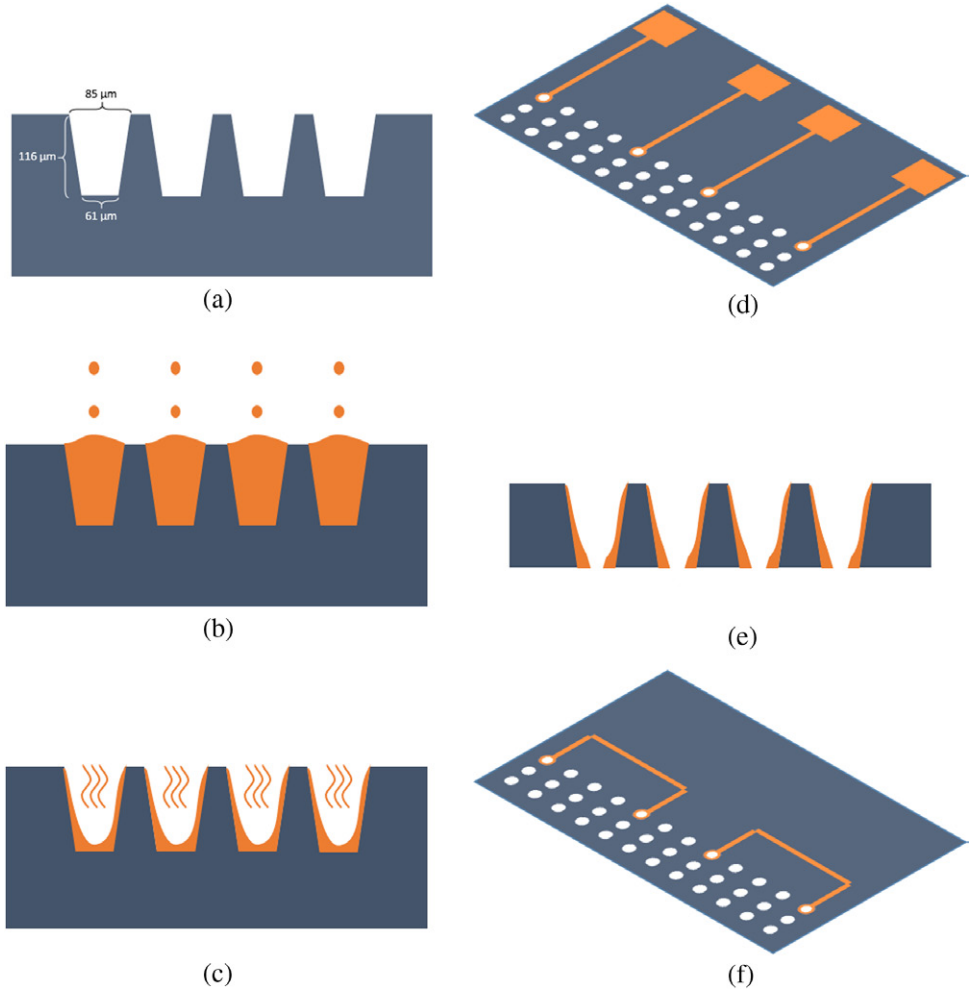

Figure 2. Inkjet printed TSV fabriction process. (a) Via-hole fabrication on silicon. (b) Via filling with ink. (c) Solvent evaporation and sintering of nano-metal. (d) Printing and sintering conductive routes between the metallized vias and measurement pads. White dots represent the vias viewed from the top. (e) Thinning to 100 μm. (f) Printing and sintering conductive routes between the metallized vias on the back side. The white dots represent the vias viewed from the bottom after the thinning.

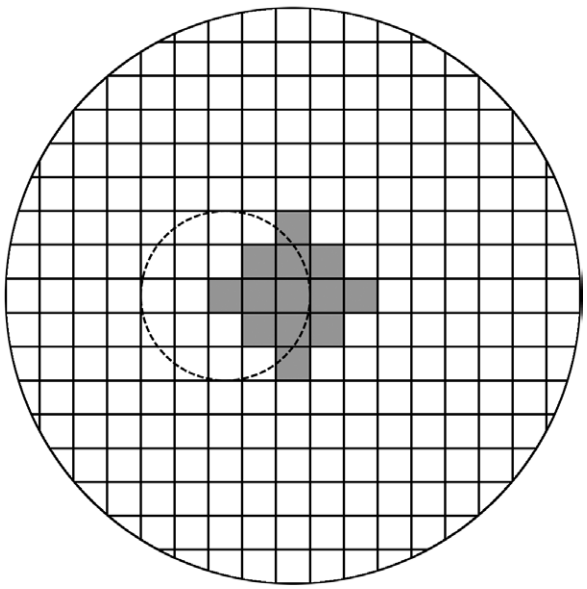

Figure 3. The pattern used for the printing (5080 dpi). The grey pixels in the middle of the pattern represent the center of droplets. The circle shows the size of the via and the dashed circle indicates drop-size at air.

in section 2.1), (b) via filling with ink, (c) solvent evaporation and sintering of nano-metal, (d) printing and sintering conductive routes between the metallized vias and measurement pads, (e) thinning, and (f) printing and sintering conductive routes between the metalized vias on the back side. In this research, we used silicon chips (size of 2 cm $\times$ 2 cm) instead of full wafers.

At the beginning a pattern with 13 droplets (figure 3) was printed to fill the via holes. From our previous experience with partial metallization of these vias we found that the adhesion of the silver layer after sintering to the sidewall is good enough; therefore, before printing no specific treatment was done to the via sidewalls. The printing plate was heated up to 60 °C and no delay was set between the printing of the layers. Since the volume of each droplet is 10 picoliter, without considering the solvent evaporation, 196 droplets or 15 layers are needed to fill the vias at first place (figure 2(b)). However, more ink (20 layers) was intentionally printed to have a controlled overflow and enough material coverage at the sharp edge of the vias in order to ensure good electrical connection over the edge.

After filling the vias, the sample is placed in convection oven heated to 220 °C for 1 h as recommended by the ink

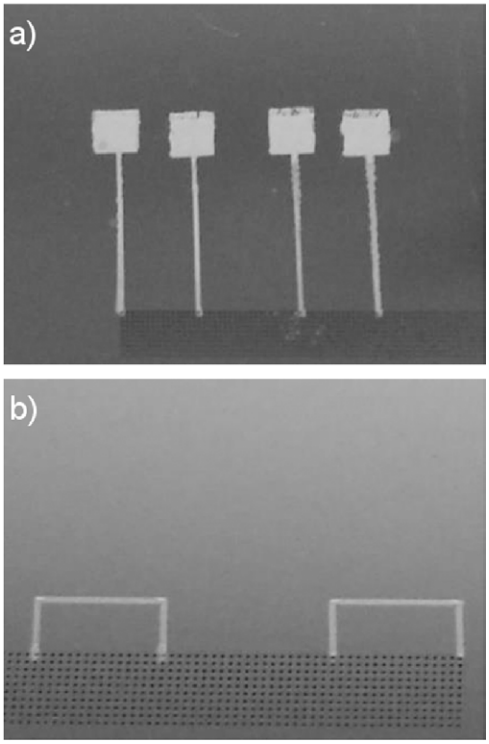

Figure 4. Top (a) and back side (b) of the final fabricated sample.

manufacturer [13], and taking into account our previous study on oven sintering process optimization for inkjet-printed Ag nanoparticle ink [15]. In the sintering process, first the solvent (figure 2(c)) and dispersant material around the nanoparticles evaporate and then, because of partial melting and welding of nanoparticles, a uniform conductive layer will be formed [15].

Forth step is fabrication of the top metal layer. On top side, the edges of the vias were separately connected to the designated printed pads via a printed conductive path (figure 2(d)). Samples were sintered (220 °C, 1 h) after the printing.

The Nnext step was the thinning of the samples (figure 2(e)). The samples were thinned to 100 μm to reveal the bottom of the blind vias. The thinning was done by IMEC.

At the final step, the end of each pair of the vias was connected on the back side by the inkjet-printed conductive route (figure 2(f)). Samples were again sintered in the same way. Figure 4 shows the top and back side of the final fabricated sample for the electrical characterization.

4. Results and discussion

The resistances of the samples were measured separately using two designated probe pads as shown in figure 5. One test sample contains top (two pads and lines length of 5 mm and width of 100 μm) and bottom (line length of 4 mm and width of 100 μm) metals and two TSV structures. An acceptable resistance of 8.8 ohm for the test structure was measured because of the good connection of the conductive routes at the back side to the inner coverage just at the bottom of the vias (~5 μm and ~7 μm) as shown in figure 6. Considering the resistance of the routes on both sides of the chips and also that

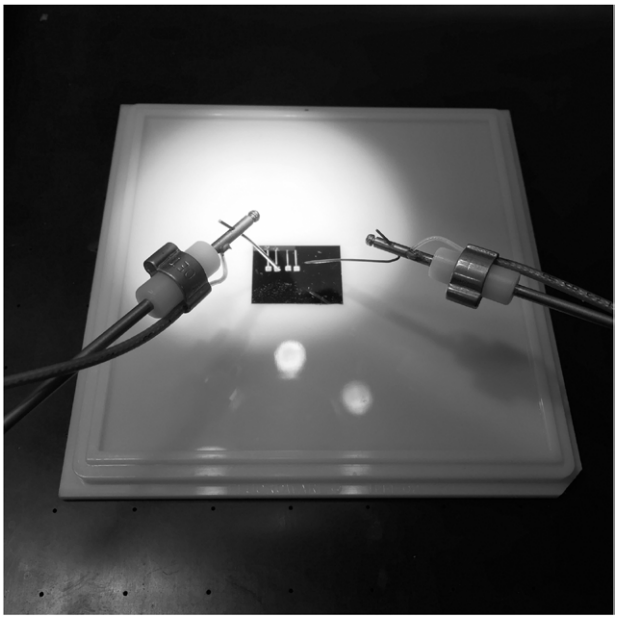

Figure 5. Measurement setup for the electrical characterization.

both of the vias have equal resistance, it was deduced that the resistance of a single via in this case could be less than 4 Ω.

In addition to a good connection at the end of the vias, there is another critical part at the edge of the vias (top side) which is needed to be well connected to the route. In order to do this, first, the coverage at the top should be adjusted to be thick enough and second, there should be an intentional overflow so that the inner coverage at the edge is connected to the surface of the chip where the routes are printed afterwards to make the link to the pads.

Figure 7(a) shows the SEM micrograph and optical microscope picture (on the lower-left corner) of a blind via after printing 15 layers and sintering with good coverage on side walls. The gap at the bottom of via could be attributed to the poor adhesion, ink shrinkage or dicing process. It is not a problem in this case since the bottom of the via will be removed in the thinning process; but the coverage at the top edge of the via is not suitable enough to be connected to the route on the surface. On the other hand, figure 7(b) shows the SEM micrograph of the coverage both on the side wall and the sharp edge of the thinned via which was used for the resistance measurement. As marked, by printing 20 layers into the via and conductive route on the surface, a perfect connection was made successfully at the edge between the wall coverage and top side coverage, which is essential for linking the vias to the probe pads.

5. Conclusion

In this work we demonstrated a partial metallization of via side walls (using inkjet and nanoparticle ink) and the electrical characterization of the vias filled using this approach. It was concluded that the resistance of a single via is in the range of less than 4 Ω. In addition to this, it was realized that the challenges in the fabrication process needed for the electrical measurement were the need to have a good coverage at the edge and bottom (after thinning) of the vias.

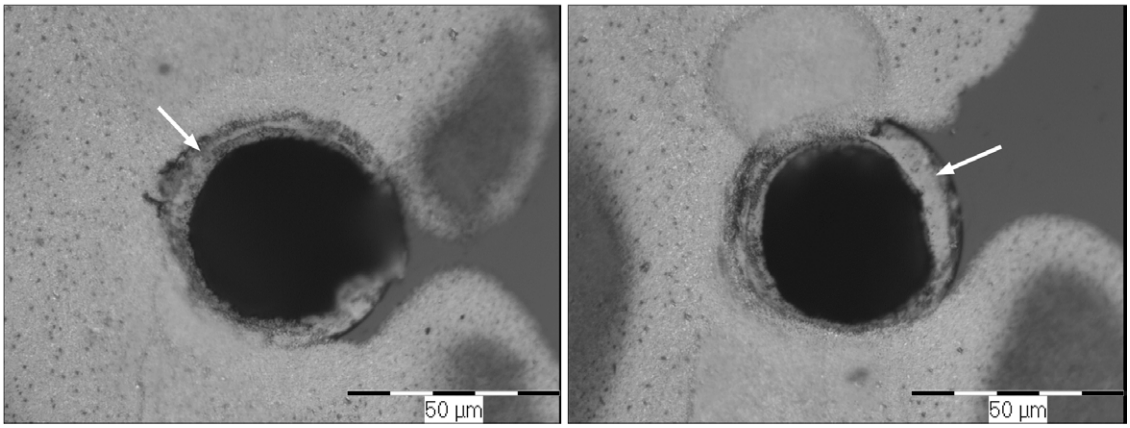

Figure 6. Inner coverage (shown with arrows) at the bottom of the thinned vias.

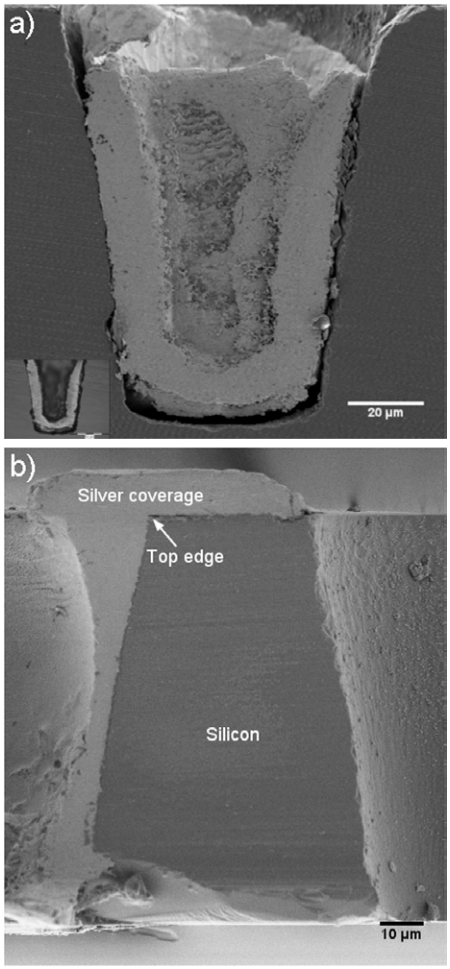

Figure 7. (a) SEM and optical micrographs of a blind metallized via, and (b) SEM micrograph of a thinned metallized via.

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