

Study of Diebond Machine Platform on Theta Rotation Performance

Edwin M. Graycochea Jr.^{1*}, Rennier S. Rodriguez¹ and Frederick Ray I. Gomez¹

¹*New Product Development and Introduction, Back-End Manufacturing and Technology
STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.*

Authors' contributions

This work was carried out in collaboration among the authors. All authors read, reviewed, edited and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2021/v20i817357

Editor(s):

(1) Dr. Guang Yih Sheu, Chang-Jung Christian University, Taiwan.

Reviewers:

(1) Regna Tri Jayanti, Metal Industry Polytechnic of Morowali, Indonesia.

(2) Mohammad Alibakhshikenari, University of Rome Tor Vergata, Italy.

Complete Peer review History: <http://www.sdiarticle4.com/review-history/68059>

Original Research Article

Received 05 April 2021

Accepted 10 June 2021

Published 14 June 2021

ABSTRACT

Theta rotation on die during diebond process is one of the critical machine responses especially for land grid array (LGA) device with tight tolerances requirement. The paper focuses on the die theta rotation tolerance capability with critical design for LGA device evaluated on two different diebond machine platforms. The evaluation was narrowed down into two main diebond machines with the objective of attaining the best performance in terms of die theta rotation tolerance capability. The study used a side-by-side comparison analysis in terms of theta rotation on the two machines and presented the effect of machine selection on the theta rotation response. Theta rotation was monitored and both machines satisfied the specification of 1 degree of maximum rotation, though diebond Machine 1 was able to produce a more stable diebonding with only around less than 0.15 degree of theta rotation variation. For future works, the selected diebond machine could be used for devices with critical requirement.

Keywords: Diebond process; LGA; semiconductor; theta rotation.

*Corresponding author: Email: edwin.graycocheajr@st.com;

1. INTRODUCTION

Die attach or diebonding is the process of attaching a semiconductor die either a leadframe or substrate carrier material. The process starts with picking the semiconductor die from a wafer silicon tape. The typical flow in diebonding is: first, the ejector needle pushes up the target Silicon die from the wafer Silicon tape; then is picked by a rubber-tip or pick-up tool; next is placed and aligned die with respect to the die paddle of the leadframe or substrate carrier material; and lastly the standard die bonding techniques, bond force and ultrasonic. Land grid array (LGA) substrate packaging technologies are continuously developed and improved to deliver high quality and robust products for various applications. A common direction of semiconductor manufacturing companies is to increase the manufacturing yields and maintain high quality while minimizing the wastage and assembly rejections. Challenges in assembly manufacturing are inescapable especially with the new and continuous technology trends and breakthroughs [1-5]. In this paper, a LGA device is identified to be critical due to the theta rotation response especially with a critical design. When the package has a requirement, the die must be placed properly on the carrier, for this case the

substrate, using a diebond process. Fig. 1. shows the representation of the device with theta rotation. The substrate is the carrier where the Silicon die is attached. The lead fingers on the substrate would provide the connection from the die through the wirebond and into the input/output (I/O) LGA pads at the bottom of the substrate. Theta rotation is the non-ideality response of the die during diebonding process in terms of the die rotation with respect to the center.

To guarantee its integrity, during production run, diebond process is incorporated with multiple criteria such as, die placement, bond line thickness, die shear test, peel off and epoxy voids. Die placement is a critical criterion in diebond process because this can check the actual die placement requirement of the device and to verify if the machine can meet the die placement requirement.

Assembly process flow for LGA device is shown in Fig. 2. highlighting the assembly process in focus. Important to note that assembly process flow changes with the product and the technology. Also as previously mentioned, new technologies and breakthroughs bring along its many challenges.

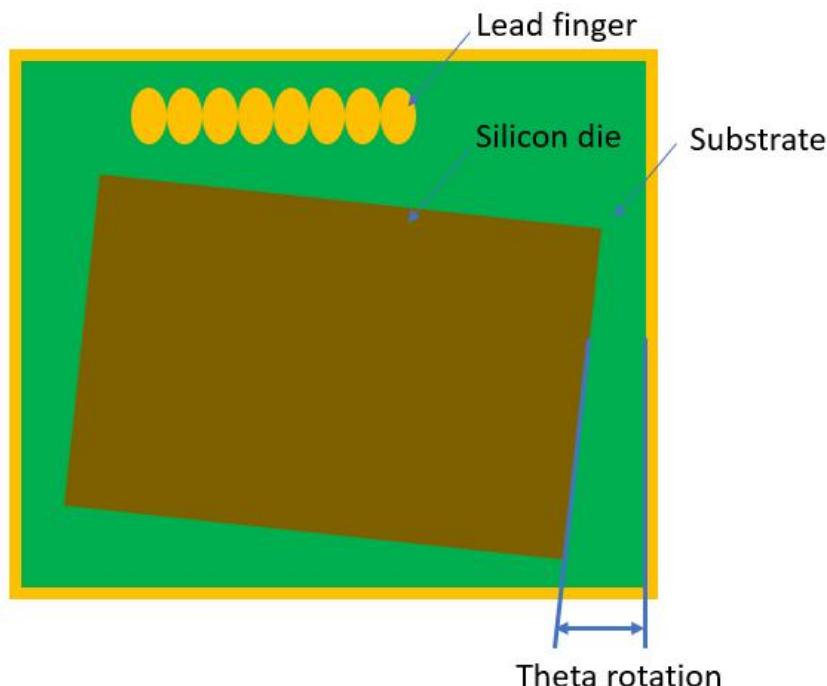


Fig. 1. Actual device with theta rotation

Theta rotation LGA device are critically monitored as this may lead to exposed die on the package and wire to wire shorting on wirebonding process. Exposed die in semiconductor packages often happens within the package itself, which caused by shifting the silicon die outside the required theta rotation capability on the desired machine. Exposed die is detected during the cutting of units individually at singulation process. Wire to wire shorting is another critical response if the theta rotation played outside the machine capability and this can be a failure during reliability testing.

Usually, a tight theta rotation and its tolerance is necessary on devices with very tight design clearances. Tight clearance in a semiconductor package is a big challenge in assembly manufacturing especially for the very small packages. Clearance is a critical factor during IC assembly since the distances and spaces between individual parts are used to anticipate the variation or deviation produced by the individual process step during assembly. Moreover, each assembly process is affected by the equipment and material tolerances.

2. METHODOLOGY

The LGA device was evaluated in two different diebond machine platforms for critical design to meet the theta rotation capability. Machine 2 is an older version that has a tolerance capability of 2 degree using a die attach film (DAF) material. The large tolerance means that the theta rotation is not stable or robust during the attachment or bonding of die on the substrate. In contrast, Machine 1 is capable to achieve 1 degree

tolerance, which is relatively better than previous one.

The data gathering flow is defined in Fig. 3. The wafer is taped to protect the front side layer during back lap process. The wafer is then grinded to 70 microns final die thickness. The sawn dice were taped in wafer ring are later transferred to diebonding station for setup and optimization. Technician is responsible to perform a pre-buy-off to measure the necessary requirement of the device. The bonded units are then subjected pc buyoff, to check all the gating criteria, if one of the requirements is failed, the units are returned to the technician and adjust the parameter corresponds to the failed criteria.

3. RESULTS AND DISCUSSION

The side-by-side analysis of theta rotation of the two diebond machine platform is shown in Fig. 4. This data is coming from the machine that has an actual reading during the diebond process. Both machines achieved the specification of 1 degree of maximum theta rotation. Diebond Machine 1 has a more stable diebonding response with only around 0.1 to 0.15 degree of theta rotation, while Machine 2 has a larger range of response. Though all machines satisfied the specification, lower theta rotation deviation is preferred for devices with tight clearances and critical requirements. Normally, the measurement is based on the wiring layout if there is a specific measured requirement. Machine 1 was able to run this type of new technology with critical criteria on the theta rotation capability with less variation.

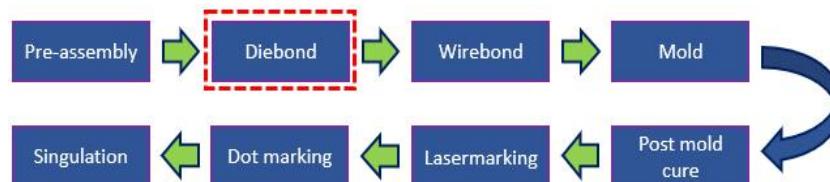


Fig. 2. Actual process flow for LGA device

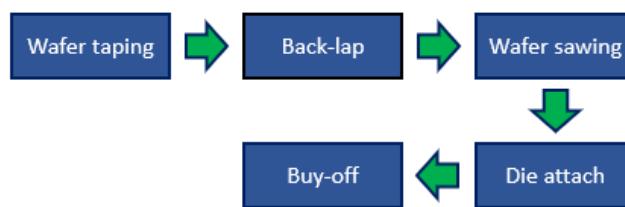


Fig. 3. Data gathering flow

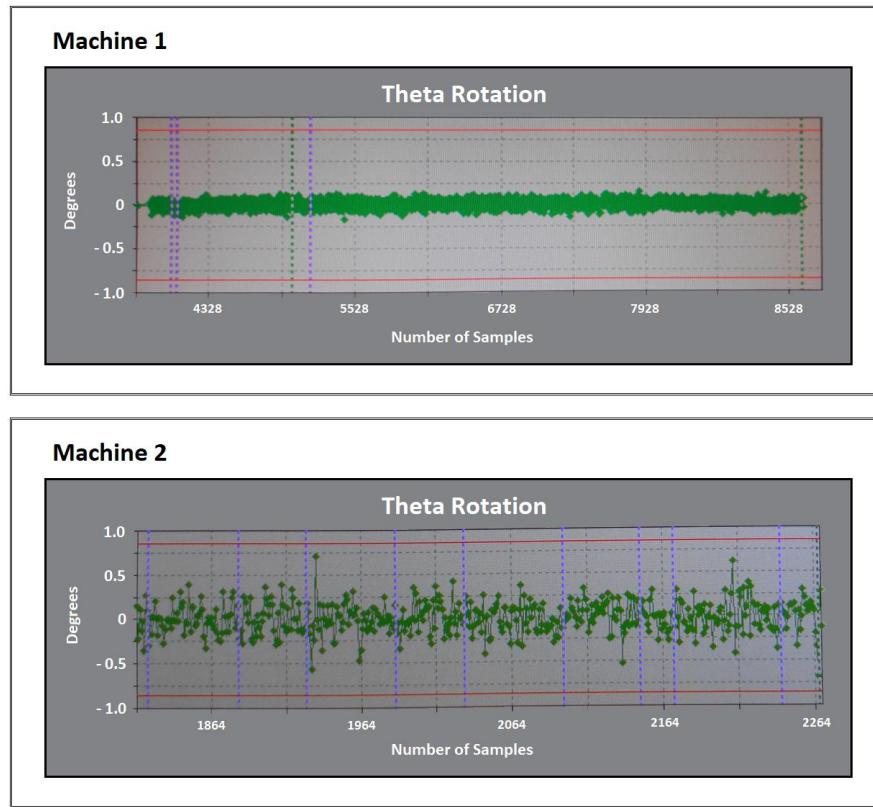


Fig. 4. Side-by-side analysis of theta rotation on two diebond machines

4. CONCLUSION AND RECOMMENDATIONS

The paper discussed the evaluation of different machine platforms where to run the critical devices with tight die placement tolerance capability especially for LGA devices. In this study, it has been shown that Machine 1 has a significant difference in attaining the best theta rotation.

With this, Machine 1 is capable for critical and tight die placement requirement especially for newer semiconductor packaging technologies. For future works, Machine 1 could be used for such devices with critical bonding diagram requirement. Moreover, works and studies shared in [6-11] would help reinforce the robustness and optimization of diebond process.

ACKNOWLEDGMENT

The authors are greatly thankful to the New Product Development & Introduction (NPD-I) colleagues and the Management Team for the continuous solid support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
2. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
3. Xian TS and Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.
4. Greig WJ. Integrated circuit packaging, assembly and interconnections. 1st ed. USA: Springer; 2007.
5. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process

- control. 1st ed., Wiley-IEEE Press, USA; 2006.
6. Buenviaje Jr. S, et al. Process optimization study on leadframe surface enhancements for delamination mitigation. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;95-100.
7. Bacquian BC, et al. Bond line thickness characterization for QFN package robustness. Journal of Engineering Research and Reports. 2020;14(2);15-19.
8. Abdullah Z, et al. Die attach capability on ultra thin wafer thickness for power semiconductor. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference. Malaysia: 2012;1-5.
9. Rodriguez R, et al. A study of dispense needle for die attach voids mitigation. Journal of Engineering Research and Reports. 2020;14(1);25-29.
10. Chin LS, et al. Epoxy die attach challenges in miniature and compact DFN/QFN packages. IEEE 10th Electronics Packaging Technology Conference (EPTC). Singapore. 2008;475-480.
11. Sumagpang Jr. A, et al. Introduction of reverse pyramid configuration with package construction characterization for die tilt resolution of highly sensitive multi-stacked dice sensor device. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;140-146.

© 2021 Graycochea et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (<http://creativecommons.org/licenses/by/4.0>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:
The peer review history for this paper can be accessed here:
<http://www.sdiarticle4.com/review-history/68059>